Design of CMOS Integrated Circuits for Full-Duplex Radios

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Design of CMOS Integrated Circuits for Full-Duplex Radios

A

Thesis submitted

for the award of the degree of

DOCTOR OF PHILOSOPHY

By

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DEPARTMENT OF ELECTRONICS AND ELECTRICAL ENGINEERING

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APRIL 2021

Declaration

This is to certify that the thesis entitled "**Design of CMOS Integrated Circuits for Full-Duplex Radios**", submitted by me to the Indian Institute of Technology Guwahati for the award of the degree of **Doctor of Philosophy** is a bonafide work carried out by me under the supervision of **Dr. Nagarjuna Nallam**. The contents of the thesis, in full or in parts, have not been submitted to any other University or Institute for the award of any degree or diploma.

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Certificate

This is to certify that the thesis entitled "**Design of CMOS Integrated Circuits for Full-Duplex Radios**", submitted by **Prateek Kumar Sharma** (156302010), a research scholar in the *Department of Electronics and Electrical Engineering, Indian Institute of Technology Guwahati*, for the award of the degree of **Doctor of Philosophy**, is a record of original research work carried out by him under my supervision and guidance. The thesis has fulfilled all requirements as per the regulations of the institute and, in my opinion, has reached the standard needed for submission. The results embodied in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

Dated:

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To

My parents

for their love and sacrifice

Acknowledgments

I always believe that "one should not only follow his dream, but also fulfill the dreams that your loved ones have seen for you".

First of all, I want to thank my supervisor Dr. Nagarjuna Nallam, who is a great mentor. I learned a lot of things from him. I can not even imagine this journey without him. After my bachelor's, I was nothing in terms of technical aspects related to integrated circuits. In my initial days of Ph.D., he sat beside me in the lab and simulated various ideas. He even worked late at night many times whenever it was required. He always motivated me to think big. Because of him, I have submitted many papers in some renowned conferences and journals without the fear of rejection. Whenever there was some rejection, he used to encourage me. We used to discuss the different ideas in the lab and always try to give tough competitions to our peers. He always believes in perfection. We used to spend a lot of time while writing technical papers. He always tells me to criticize your work to know your reviewer's perceptive. I am very grateful to my supervisor for his guidance and support throughout my journey. I would like to thank Professors H.B Nemade, K.R Singh, Himangee Kapoor for being on my doctoral committees. I appreciate their time and effort in evaluating my progress and providing valuable comments.

This journey is incomplete without my friends. I have fewer friends in Ph.D., but all are very close to me. I want to thank my close friends Kamlesh, Rahul, Pralay, Indrajit, Satyajit, Tasleem and Himakshi. I shared a lot of enjoyable moments with them. I want to thank Kamlesh and Dada (Indrajit) for their valuable technical discussion. We worked day and night in the lab during my tapeouts. Without their help and efforts, it would not be possible. I want to give credits for all my achievements during my Ph.D. I learned a lot of things from both of you. I have seen him working continuously in the lab without any breaks. I am always admired by Dada's patience. I have never seen him tensed. I will miss those moments when Kamlesh and I used to make fun of Dada. During my initial days of Ph.D., the first person I interacted with most is Rahul bhai. I have completed my course work with him. It is actually from the classroom where our friendship has started. I can say he is the most sensible person in our group. He has various things to do in his routine such as running, meditation, playing, etc. I will miss the discussions with Pralay bhai related to politics and other

issues. In the lab, we used to have high-level talks surely not related to technical stuff. Satyajit is the master chef of our group. We used to party in his room where, he cooks different dishes for us. He is always in a happy mood. The person who is tortured all the time is Tasleem bhai. He is the one who makes the lab lively. We crack jokes on him. I surely will miss those moments. Himakshi is a cheerful person. None one can feel bored in her presence. She is my good friend and kind-hearted. She used to come to our lab and light the tensed environment. I will miss those days. And of course, I will miss all-party moments with Kamlesh, Pralay, Dada and Himakshi. I thank to my VLSI lab seniors Vinaya, Saroj, Brijesh, Rajan, Pavan, Karam, and Hari for their guidance and support. I want to thank other lab members, Vimal, Mridul, Deepjyoti and Hari.

Today whatever I am, because of my parents and their upbringing. My father is my inspiration. As head of the family, he has fulfilled all our needs. Whatever he earned, he used to spend on my brother and on me. He always supported me a lot for my education. I think without his sacrifice, this journey will not complete. My mother is a mentally strong lady. In my childhood, she used to take care of me, especially when my father was posted to different places. She always taught me moral values. I can never forget her teachings. I have no words to describe my parents' love and emotions. I want to thank God for having such parents. I wish I can become a good son and take care of them in the future. My elder who always support me in difficult times. He guides me on the best career options. As an elder brother, he fulfills all responsibilities of the family. I am thankful to my Nanaji and Naniji for their blessings and support.

I want to thank a special person who came into my life and shared the most beautiful moments of my life. I am always thankful to her for transforming me and for what I am today. There was a time when I got engaged in my work. I did not have time for anyone, even sometimes not for my family members. That person taught me how to live your life for someone else. Because of her, I realized the importance of your loved ones. We come across many people in our life, but there are few whom you always want to remember. I always cherish those joyful moments and events wherever I will go. Finally, I pray for her happiness and good life.

Prateek Kumar Sharma

Abstract

In-band Full-duplex (FD) radio is an emerging technology, which transmits and receives the signal simultaneously at the same frequency. FD has the potential of doubling the throughput with low latency. The main challenge associated with an FD system is the self-interference (SI). The SI in an FD radio is caused by the leakage and the echo signals from the transmitter to its own receiver. Due to the direct or the parasitic path, the transmitted signal gets leaked into the receiver in an FD radio. Whereas, an echo signal occurs due to the reflection of the transmitted signal in free space. The large in-band SI signal makes the demodulation of the weak desired signal a hard task.

To mitigate the problem of SI in an FD radio, an SI canceling circuit which generates an SI canceling signal is often used. The SI canceling circuit should be capable of providing variable attenuation, variable time-delay, and variable phase delay. Apart from the SI signal, blockers from different bands can degrade the performance of the FD receiver, especially in the sub-6 GHz range. The main objective of this research is to investigate the fully-integrated circuit techniques for SI cancellation in FD receivers.

The following three modules have been proposed, in this thesis, for FD radios: (a) A transformer-less duplexer using two-port N-path Balun, (b) A passive continuous charge-sharing vector modulator, and (c) A second-order baseband noise-canceling TIA for enhanced linearity and low noise performance. The proposed transformer-less duplexer uses two 2-port N-path bandpass filters to form a balun that rejects the same-channel transmitter leakage into the receiver. N-path BPFs in the receiving path offer high-Q filtering and tunability. The duplexer has >55 dB of transmitter-to-receiver isolation, <6 dB of transmitter-to-antenna insertion loss (IL) and < 7 dB of antenna-to-receiver insertion-loss, in post-layout simulations, with no additional tuning at any of the 50 Ω ports.

The passive vector modulator (VM) presented in this work provides simultaneous down-mixing, attenuation and phase-shifting. The VM is used to generate the SI canceling signal

for SI cancellation. A prototype FD receiver including the proposed VM is implemented in CMOS 130 nm technology. The receiver is tunable from 0.1 GHz to 0.95 GHz. In FD mode at 900 MHz, the receiver has an effective input-referred third-order intercept power (IIP3) of +7 dBm, SI-to-noise-and-distortion-ratio (SINDR) of ≈ +65.3 dB at -27.5 dBm SI in 15 MHz bandwidth, and noise figure (NF) degradation of less than 1 dB.

Both of abovementioned SI canceling circuits are passive and are compatible with passive mixer-first receivers. The proposed SI canceling circuits are also highly linear as they consist of only passive switches and capacitors. Moreover, they do not contribute much noise to the system. The IIP3 and NF of the system are mainly limited by the receiving path rather than the SI canceling path. To improve the performance of the proposed FD receiver, a second-order baseband noise-canceling (NC) scheme is proposed. A prototype of the mixer-first receiver using the proposed TIA is implemented in CMOS 180 nm technology and tested in the laboratory. In measurements, the receiver achieves an NF less than 4 dB and IB-IIP3 of +14.5 dBm over a frequency range of 0.2-to-1.2 GHz. The measured OB-IIP3 is +25 dBm at a frequency offset of 2.2 times the bandwidth while consuming a static power of 20 mW. All these results are presented in this thesis.

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Introduction

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1.1 Introduction

With the evolution of wireless communications, the demand for high-speed mobile data is increasing. Fig. 1.1 shows the growth in mobile data traffic [1] in recent times. From Fig. 1.1, mobile data traffic is expected to reach 77.49 exabytes per month by 2022. The next-generation wireless standard (5G) is expected to support such high data traffic with data rates of more than 1 Gbps. 5G wireless standard has to support three major application categories: enhanced mobile broadband, ultra-reliable low latency communications, and massive machine to machine communications. For a mobile user, the demand for high-definition video streaming can be achieved using next-generation systems. For industrial and healthcare applications, an ultra-low latency network in the order of 1 ms can be fulfilled using 5G. Due to low latency, 5G can make augmented reality and virtual reality applications, both immersive and far more interactive. 5G connects a massive number of sensors virtually, providing extremely reliable and low-cost connectivity solutions for Internet-of-Things (IoT).

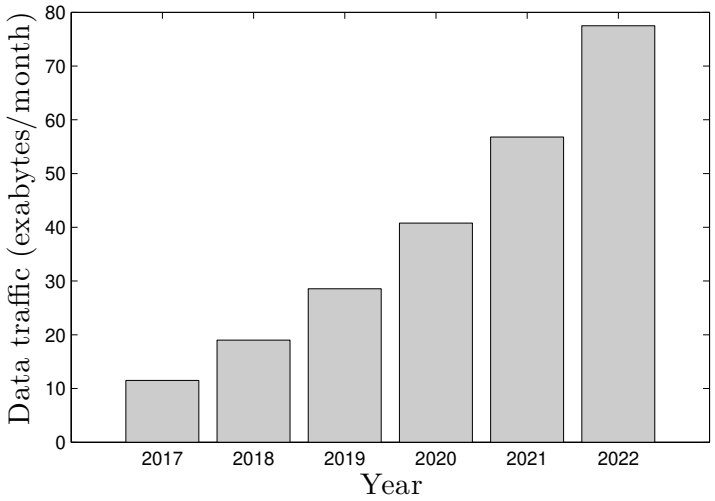


Figure 1.1: Global mobile data traffic.

The next-generation wireless communications promise an exciting future, but at the same time, it imposes several strict requirements. Even though a large spectrum is made available at millimeter wave frequencies, there is a severe spectrum congestion at sub 6 GHz frequencies. The techniques to relax these spectrum issues and achieve a high data rate for 5G are beamforming, massive Multiple-Input-Multiple-Output (MIMO), and full-duplex (FD) wireless communication.

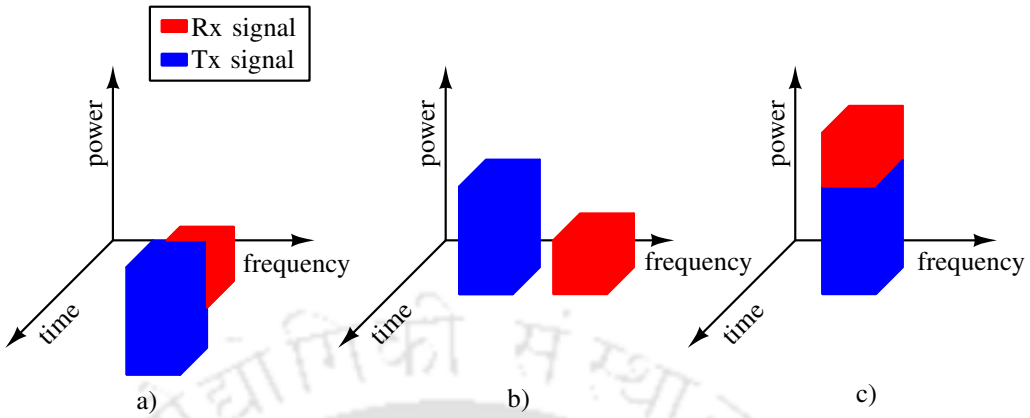


Figure 1.2: Transmit and Receive signal in (a)Time-division-duplexing (TDD), (b)Frequency-division-duplexing (TDD), and (c)In band FD.

1.2 Full-duplex system

In-band (IB) FD communication is an emerging technology, which allows simultaneous transmission and reception at the same frequency. Traditional wireless links distinguish the transmit and receive signals on the Physical layer (PHY), using time-division-duplexing (TDD) or frequency-division- duplexing (FDD). The comparison of transmitting and receiving signal spectra in TDD, FDD, and IB FD is shown in Fig. 1.2. In the PHY, FD offers up to 2× spectral efficiency. In [2], different network concepts have been developed to exploit FD capabilities in wireless communication radios, which improve user access. In cellular applications, FD can mitigate some fundamental problems like hidden terminals, bandwidth degradation, and network latency for access points and mesh networks. Other advantages of FD include collision prevention, low latency, and security.

There are many challenges in the implementation of IB FD radio [3]. The major issue is a strong IB self-interference (SI) signal from the transmitter to the receiver. The SI signal is caused by the leakage and echo signals from the transmitter to its own receiver. In an FD radio, the transmitter leakage is caused by the on-chip or on- board parasitic paths between the transmitter and the receiver. The coupling is also caused due to shared antenna interface. A transmitter echo is an attenuated, delayed, and phase-shifted version of the transmitted signal which enters the receiver from free space. It is difficult to demodulate the desired signal (much weaker) in the presence of a strong SI signal. Fig. 1.3 shows a typical FD receiver. The difference in power levels of SI and received signal is shown in Fig. 1.3.

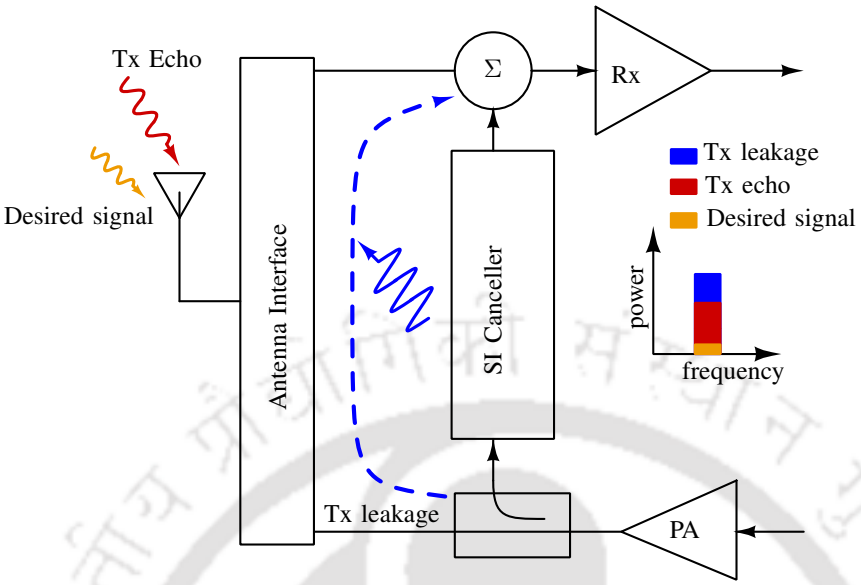


Figure 1.3: Self interference in FD radios.

In a two-antenna system, the transmitter leakage is usually very low at radio frequencies but could be very high at millimeter-wave frequencies due to the proximity of the transmitting and receiving antennas. In a single antenna system, transmitter leakage can be reduced by using an electrical balanced duplexer (EBD) [4–8] or a circulator [9–11]. One way to mitigate the problem of SI is to create an SI canceling signal that will nullify the SI present in it when combined with the received signal. A canceller signal can be generated by tapping a copy of the transmission signal and adjusting its amplitude, delay, and phase. Therefore the SI-canceling circuit that generates the canceller signal should be capable of providing a variable attenuation, a variable time delay, and a variable phase delay. In narrow-band systems, the effect of group delay can be approximated by phase delay. In wide-band systems, a group delay causes frequency dependent phase delay for SI signal. The effects of delay and phase mismatches are further discussed in Chapter 3.

1.3 Full-duplex requirements

As discussed in the previous section, one needs to tap the transmitted signal to generate an SI canceller signal. The transmitted signal can be tapped from any of the three different domains in the transmit path: a digital transmitted signal, an analog baseband signal, or an RF signal. Three possible SI canceller architectures can be derived, as shown in Fig. 1.4, based on the location of the TX

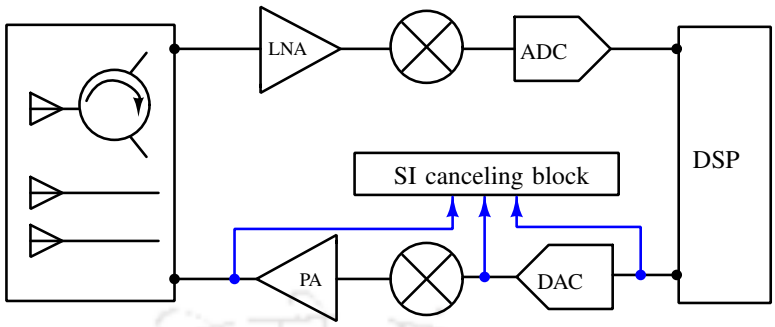


Figure 1.4: SI canceller architectures with different locations of TX tapping.

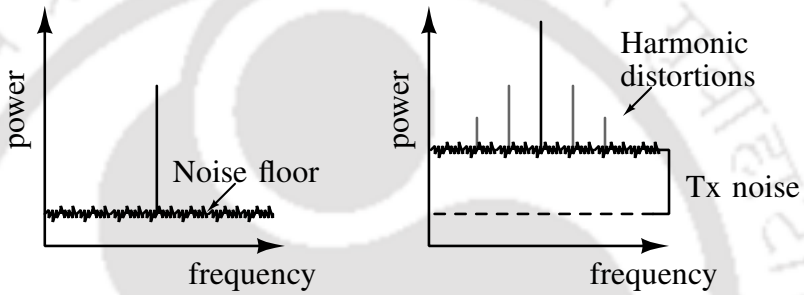


Figure 1.5: (a) Ideal transmitted signal and (b) actual transmitted signal.

tapping. The spectrum of the transmitted signal in these three domains will have different components due to the nonidealities of the individual blocks. For example, Fig. 1.5(a) shows the spectrum of the TX signal in the digital domain, and Fig. 1.5(b) shows the spectrum of the same signal at the output of the PA. The signal in Fig. 1.5(b) includes the harmonics due to the PA nonlinearity. Also, all the signal processing blocks in the transmit path will contribute noise to the output spectrum. The oscillator phase noise also raises the noise floor of the upconverted TX signal. The transmitter echo may contain all these nonidealities due to the PA, oscillator, and mixer blocks. The nonlinearities of the echo signal can be canceled only if the SI canceling signal also contains these nonlinearities. Therefore, the SI canceller should use the output of the PA signal for generating the SI canceling signal, as shown in Fig. 1.5(b). Thus, tapping the RF signal from PA output is advantageous rather than processing the analog baseband signal or the digital transmitted signal.

To understand the magnitude of SI cancellation required in a typical FD receiver, let us consider the example of a Wifi transceiver. The transmitted power in a WiFi system is +20 dBm in 20 MHz bandwidth. Assuming an isolation of 20 dB, the SI signal can be as high as 0 dBm at the receiver input. Let us also assume that the receiver has a noise figure (NF) of 10 dB. The noise floor (P_{noise})

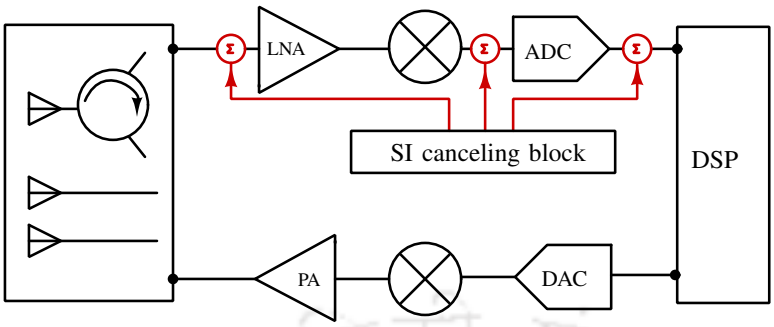


Figure 1.6: SI canceller architectures with different injecting points.

of the receiver is given by

$$P_{noise} = 10\log_{10}(kT_o) + NF + 10\log_{10}(\text{bandwidth}), \tag{1.1}$$

where T_o is absolute temperature and k is the Boltzmann constant. At $T_o = 290K$

$$P_{noise} = -174 + NF + 10\log(\text{bandwidth}) \tag{1.2}$$

$$= -174 + 10 + 73 = -91 \text{ dBm}. \tag{1.3}$$

For proper reception, one needs to attenuate the SI signal to 6 dB below the noise floor [12]. Therefore, the total SI cancellation required is 97 dB.

The canceller signal can be injected at any of the three different locations: at the input of the LNA, at the output of the mixer or after the ADC, giving three possible FD receiver architectures. Each of these three architectures has its own advantages. Cancellation of the SI at the LNA input can improve the receiver linearity. SI cancellation before the ADC can reduce the dynamic range requirement of the ADC. For SI cancellation in digital domain, the cancellation algorithm can be very complicated. Nevertheless, none of these three architectures provide the large SI cancellation required in a practical FDR (97 dB in the WiFi example discussed above). Therefore, a true FD receiver requires the combination of all these three SI cancellations, as shown in Fig. 1.6.

The SI cancellation in RF and analog domains is critical as otherwise, the receiver impairments limit the total cancellation. This is explained with the help of Fig. 1.7. As shown in Fig. 1.7, the total SI-to-noise-and-distortion-ratio (SINDR) is limited by transmitter Error Vector Magnitude (EVM) and receiver impairments if only digital SIC is adopted. Using RF and analog SIC, as shown in Fig. 1.8, can improve the receiver SINDR.

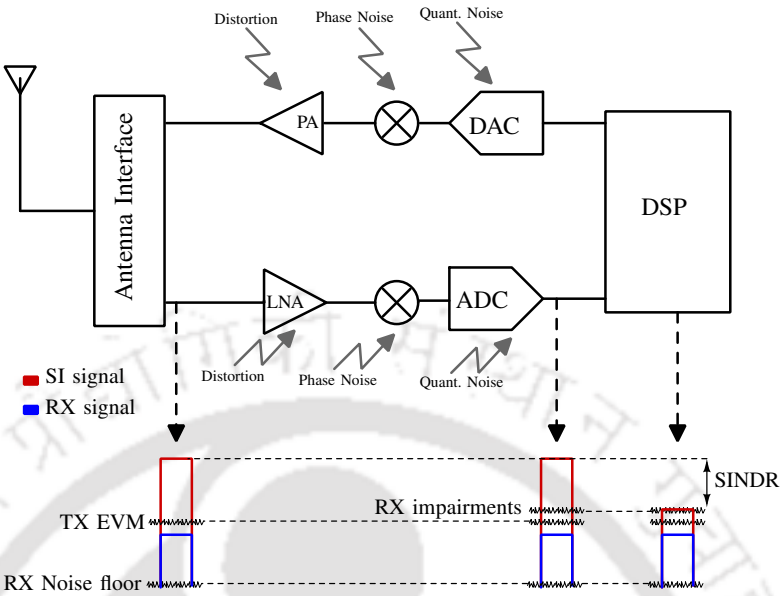


Figure 1.7: SI cancellation in digital domain.

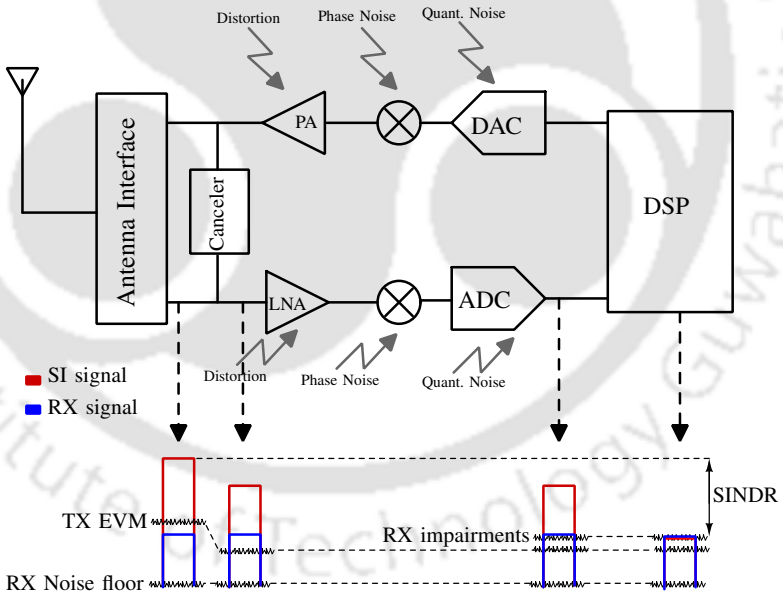


Figure 1.8: SI cancellation in both RF and digital domain.

1.3.1 Full-duplex link budget

In this section, the link budget of an FD receiver is discussed using example from Section 1.3. The objective of the link budget is to divide the total SI cancellation (SIC) required among the three cancellation stages: RF, analog and digital. From Section 1.3, the total SIC required is 97 dB.

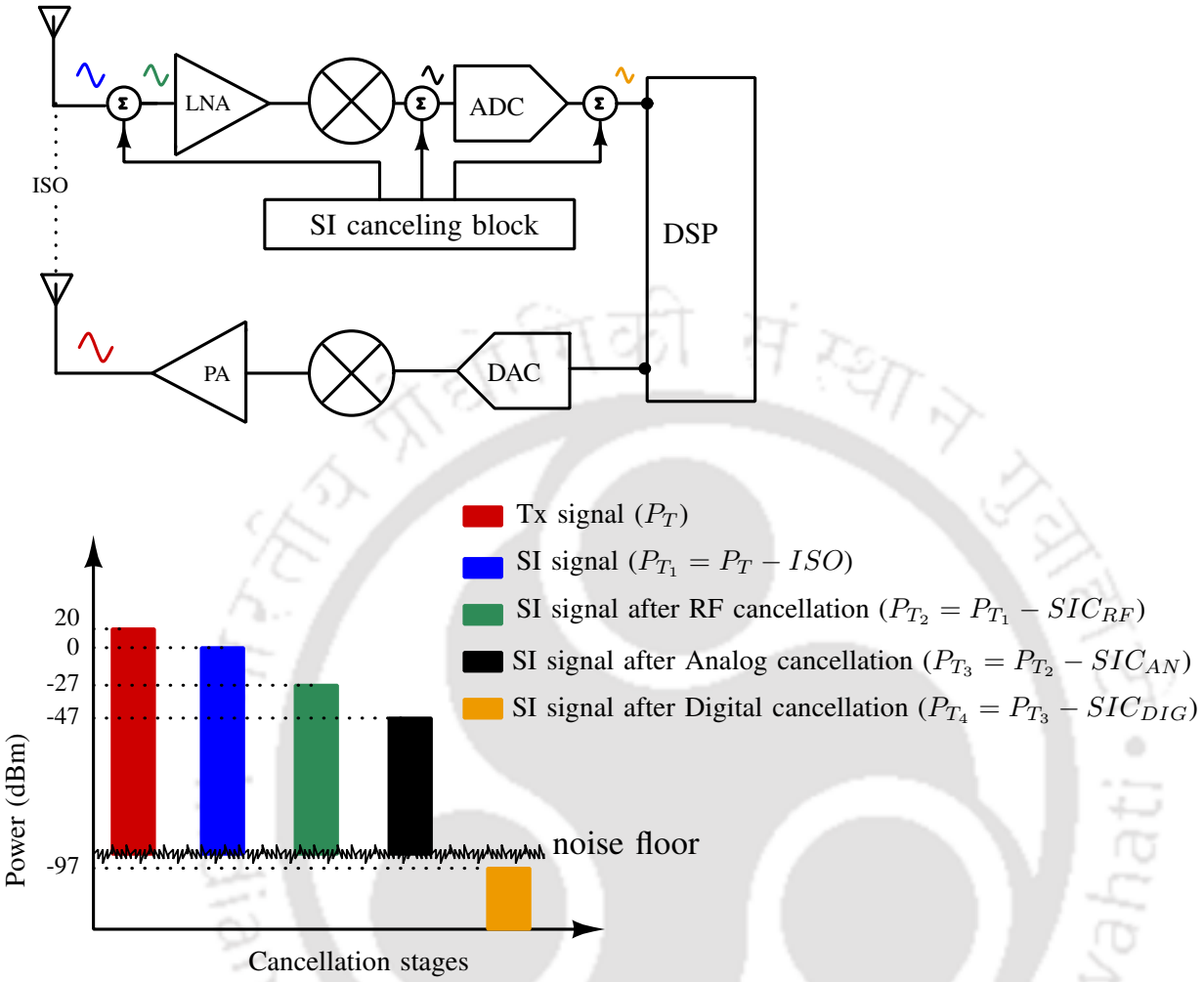


Figure 1.9: Power level of SI signal after different cancellation stages.

SI Cancellation in RF domain:

In a multi user communication system, the cross-modulation between SI and the adjacent jammer will limit the linearity of the receiver. Let us assume the following notation with respect to the figure shown in Fig. 1.9.

$IIP3_{LNA}$ is the IIP3 of LNA.

P_{in} is the power at the receiver input.

P_{CM_3} is cross-modulation signal.

P_T is the transmitter power.

ISO is antenna isolation and reflection losses.

SIC_{RF} is RF SIC.

P_{jam} is the jammer power.

P_{noise} is the noise floor.

Fig. 1.9 shows the power levels of SI after various cancellation stages. From the definition of IIP3, the IIP3 of the LNA is given by

$$\text{IIP3}_{\text{LNA}} = P_{in} + \frac{P_{jam} - P_{CM_3}}{2} \quad \text{(in dBm)}. \tag{1.4}$$

$$\text{P}_{\text{CM}_3} = 2P_{in} + P_{jam} - 2\text{IIP3}_{\text{LNA}} \quad \text{(in dBm)}. \tag{1.5}$$

The power at the receiver input after antenna isolation and RF SIC is $P_T - ISO - \text{SIC}_{\text{RF}}$. The above equation can be rewritten as

$$\text{P}_{\text{CM}_3} = 2(P_T - ISO - \text{SIC}_{\text{RF}}) + P_{jam} - 2\text{IIP3}_{\text{LNA}} \quad \text{(in dBm)}. \tag{1.6}$$

For proper reception, this inter-modulation signal should be 6 dB below the noise floor. Therefore, $\text{P}_{\text{CM}_3} = \text{P}_{\text{noise}}$-6. From (1.6), the required RF SIC can be written as

$$\text{SIC}_{\text{RF}} = P_T - ISO - \text{IIP3}_{\text{LNA}} + \frac{P_{jam} - P_{noise} + 6}{2} \quad \text{(in dB)}. \tag{1.7}$$

Let us assume P_{jam} = -33 dBm and $\text{IIP}_{3_{\text{LNA}}}$ is 5 dBm. The SIC_{RF} can be calculated from (1.7). The required SIC_{RF} is 27 dB. One can infer from (1.7) that the SIC in RF depends mainly on the linearity of the LNA and NF of the receiver. A higher linear LNA can relax the RF SIC requirement.

SI Cancellation in digital domain:

The digital cancellation depends on the dynamic range of the ADC. A 12 bit ADC may have a typical dynamic range of 72 dB [3]. Let us assume 2 bits is left for the quantization noise of ADC. The dynamic range is 50 dB for 10 bit ADC [3]. The maximum SI cancellation in the digital domain (SIC_{DIG}) can be 50 dB.

SI Cancellation in analog domain:

The remaining SIC can be implemented in the analog domain. The amount of cancellation required in the analog domain (SIC_{AN}) is 97-50-27=20 dB.

Tab.1.1 summaries the FD system link budget.

Table 1.1: FD system link budget

Specifications	Requirements	Comment
Transmitter power (P_T)	20 dBm	
Bandwidth	20 MHz	Bandwidth for LTE
Noise figure (NF)	10 dB	
Noise floor (P_{noise})	-91 dBm	Calculated from NF and bandwidth
Isolation	20 dB	Antenna isolation & reflection losses
Jammer power (P_{jam})	-33 dBm	LTE standard
Total SI cancellation	97 dB	To suppress SI below noise floor
RF SI cancellation	27 dB	Calculated from (1.7)
Analog SI cancellation	20 dB	Subtracting RF and Digital SIC from total SIC
Digital SI cancellation	50 dB	As per [3]

1.4 Objective of the thesis

The main objective of this research is to investigate the fully-integrated circuit techniques for SI cancellation in FD receivers. Recent advances in switched-capacitor circuits promise high-Q, widely tunable, and CMOS integrable RF filters. In this thesis, switched-capacitor based integrated circuits are proposed for (a) transmitter leakage and (b) transmitter echo cancellation in an FD receiver. Both of these SI canceling circuits are passive and are compatible with passive mixer-first receivers. Many on-chip SI-canceling circuits have been proposed in the recent past. [13] presents a passive and frequency tunable SI-canceling circuit based on a vector modulator (VM) downmixer. The VM downmixer is implemented with switches and capacitors. The VM presented in [13] is discrete in nature, i.e., the VM constellation consists of a few discrete points. In general, a large number of VM slices are needed to cover a sufficient number of constellation points. Moreover, the NF of the receiver in [13] degrades by more than 4 dB in FD mode. [12] presents an SI cancellation scheme based on frequency-domain equalization at RF using $G_m - C$ N-path bandpass filters. [14,15] present two-point active SI-cancellation scheme based on RF and baseband adaptive filters. The frequency range of the FD receiver in [14] is limited to 0.5 GHz (1.7-2.2 GHz) due to the limited tunability of the adaptive filters.

An ideal SI canceling circuit should be highly linear and should not contribute noise to the system. The operating frequency range of an FD receiver should not be limited by the SI canceling circuit. In this thesis, we mainly focus on the implementation of passive and frequency tunable SI canceling

blocks using switch capacitors. In such a scenario, the IIP3 and NF of the system can be limited by the receiving path rather than the canceling path. To improve the performance of the proposed FD receiver, the mixer-first receiver in the receiving path should have high IIP3 and have low NF. This thesis also proposes a second-order baseband noise-and-distortion cancellation scheme for improved linearity in N-path mixer-first receivers.

1.5 Contribution of the thesis

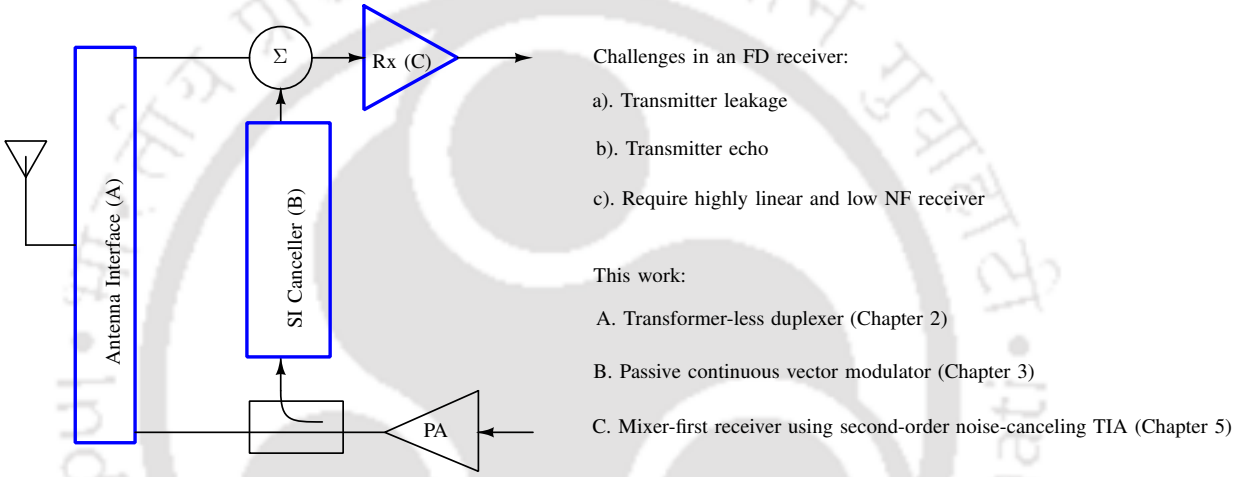


Figure 1.10: Complete block diagram of the FD transceiver (The proposed blocks are depicted with blue color).

Fig. 1.10 shows the complete block diagram of the FD transceiver where the proposed blocks are shown with blue color. The main contributions of the thesis are summarized below:

- **Transformer-less duplexer**: A transformer-less duplexer based on 2-port N-path BPFs for FD radios has been proposed in this thesis. The proposed duplexer consists of two quarter-wavelength transmission lines, and the proposed N-path balun BPF which provides an out-of-band (OB) blocker support for the receiver. A 0.45-0.65 GHz duplexer is implemented in a CMOS 65 nm technology and it occupies an active area of ≈ 0.7 mm^2.
  - **N-path balun BPF**: A widely tunable balanced-to- unbalanced (Balun) bandpass filter (BPF) is proposed using two 2-port N-path BPFs. The proposed balun uses two 2-port N-path BPFs with embedded quadrature phase shifting to achieve the single-ended to differential conversion. Analytical expressions for the IB differential to single-ended and

single-ended to differential voltage gains are derived and validated. A prototype balun is implemented in a CMOS 65 nm technology and it occupies an active area of ≈ 0.7 mm^2. Post-layout simulations show a common mode rejection of ≈ 50 dB during the DS mode of operation. During the SD mode of operation, the balun has a phase imbalance of $< 2.5^\circ$ and an amplitude imbalance of < 0.2 dB over the tuning range of 0.1-1 GHz.

- **Passive continuous vector modulator**: A frequency-agile IB FD receiver is proposed which is based on a switched-capacitor continuous-mode vector modulator. The passive vector modulator presented in this work provides simultaneous downmixing, attenuation and phase-shifting and is used to generate a baseband canceller signal for SI cancellation. A prototype FD receiver is implemented in CMOS 130 nm technology. The receiver is tunable from 0.1 GHz to 0.95 GHz. In FD mode at 900 MHz, the receiver has an effective IIP3 of +7 dBm, SINDR of +65.3 dB at -27.5 dBm SI in 15 MHz bandwidth, and NF degradation of less than 1 dB.

- **A Mixer-First Receiver With Second-Order Baseband Noise-canceling TIA**: Input-match, NF, IB IIP3, OB-IIP3 and power consumption are five crucial performance metrics of a radio frequency receiver. In a typical passive mixer- first receiver, these five performance metrics are tightly coupled with each other. In this thesis, we presented the performance tradeoffs in a typical mixer-first receiver. A second-order baseband noise- canceling TIA is presented to break the performance tradeoffs in an N-path mixer-first receiver. Analytical expressions for input impedance, NF, IB IIP3, and OB-IIP3 of the proposed receiver are derived and verified.

2

Transmitter Leakage Cancellation

Contents

2.1 Introduction

Same-channel (SC) FD radios simultaneously transmit and receive at the same carrier frequency. Simultaneous transmission and reception, with a single antenna, requires either a 3-port circulator [16] or a 4-port duplexer (or a directional coupler) at the front-end. For the on-chip implementation of FD radios, duplexers are the preferred front-end modules. On-chip duplexers are traditionally implemented using hybrid transformers [17–19]. Transformers usually occupy a large chip area, will not scale with technology, and are not tunable. Hybrid transformer based duplexers also suffer from OB interferes, in the receiving path, due to the low-quality factor of on-chip transformers.

Traditionally, transformers and baluns are designed using either lumped LC elements or transmission lines [20, 21]. Both the lumped element and transmission line approaches suffer from limited tuning capability. Recent advances in N-path circuits promise high-Q, widely tunable, and CMOS integrable RF filters [16, 22–26]. This work presents the analysis and design of a widely tunable, high-Q Balun bandpass filter. The proposed Balun is based on 2-port N-path bandpass filters and exploits their embedded phase-shifting property. This work presents a transformer-less duplexer for SC-FD radios. The proposed duplexer uses two 2-port N-path bandpass filters with embedded phase shifting [26] to form a balun that rejects the transmitter leakage into the receiver.

The rest of this chapter is organized as follows. Section 2.2 reviews the transmitter leakage canceling techniques using transformer based duplexer and N-path circulators. Section 2.3 introduces transformer-less duplexer. Section 2.4 describes a balun based on 2-port N-path bandpass filters. Section 2.5 presents a theoretical analysis of the proposed Balun N-path BPF. Section 2.6 presents a theoretical analysis of the proposed duplexer during the transmitting and receiving modes. CMOS implementation of a prototype duplexer and simulation results are presented in section 2.7.

2.2 Review of transmitter leakage canceling circuits

In this section, we will review transformer based duplexers [6, 17, 27, 28] and N-path circulator [29] for transmitter leakage cancellation.

2.2.1 Transformer based duplexers [6, 17, 27, 28]

Fig. 2.1 shows various configurations of transformer-based duplexers with four ports: transmitter (TX) port, antenna (ANT) port, electrical balance (BAL) port, and receiver (RX) port. The

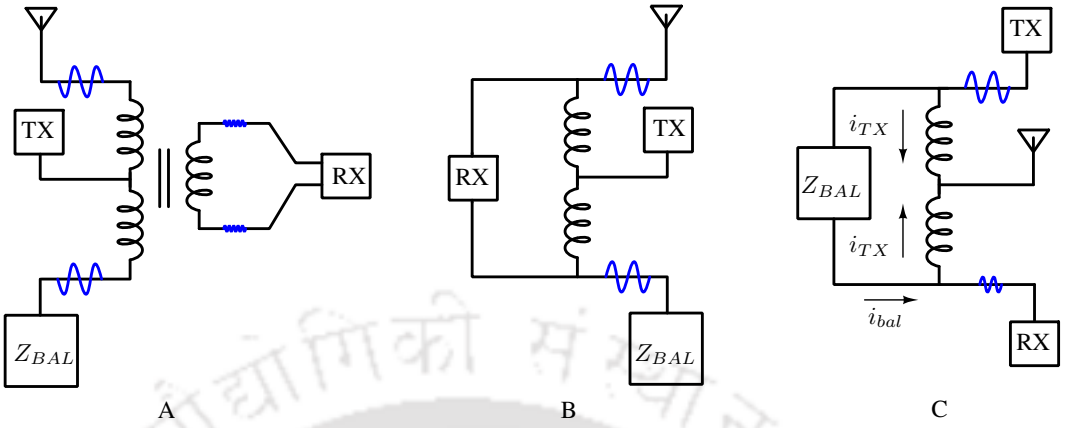


Figure 2.1: Various configurations of transformer-based duplexers.

configuration A consists of a hybrid transformer, whereas the other two are hybrid autotransformers. An autotransformer is a special case of the hybrid transformer that can be implemented using a center-tapped differential inductor. Therefore, an autotransformer can be less lossy than a two-coil transformer. However, it lacks strong common-mode suppression as compared to a hybrid transformer. In configuration A, the transmission signal is applied at the center of the primary winding of the hybrid transformer, as shown in Fig. 2.1(a). Signals with equal magnitude-and-phase at the ANT and BAL ports induce only a small common-mode signal at the differential RX port. The differential RX cancels the small common-mode signal. A hybrid transformer based duplexer is introduced in [17]. On the contrary, in configuration B, the transmission signal is suppressed only by the differential receiver. In configuration C, due to mutual coupling, the magnitude of the current flowing through the coils is the same, while the direction is opposite. Under the balanced condition, the transmission flowing through the RX port is reduced, as shown in Fig. 2.1.

In hybrid tranformers based duplexers, the transmitter-to-receiver (TX-RX) isolation depends on the matching between the antenna impedance and the balancing impedance (ZBAL). The impedance of a mobile phone antenna varies with frequency and ambient environment. This change in antenna impedance degrades TX-to-RX isolation. The TX-to-RX isolation can be improved using a tunable impedance network for balancing impedance [17]. In [27], the authors demonstrate a wideband and low-loss duplexer using an autotransformer. In this duplexer, the transmission signal swing appears as a common-mode at the inputs of the differential receiver. Due to high peak power of the TX, a large leakage signal may appear at the receiver input causing oxide breakdown in auto transformer

based duplexers. A differential version of a hybrid transformer based duplexer is presented in [28]. It enables high-power operation by improving the common-mode isolation at the cost of higher insertion loss. The limitations on the antenna impedance variation and frequency dependence remain due to the limited tunability. [6] presents a highly linear balance network that is capable of handling large transmission powers. In [6], a calibration loop is implemented to detect the TX leakage generated due to an imbalance in the duplexer and correct the balance network impedance to track antenna impedance variation.

2.2.2 N-path circulator [29]

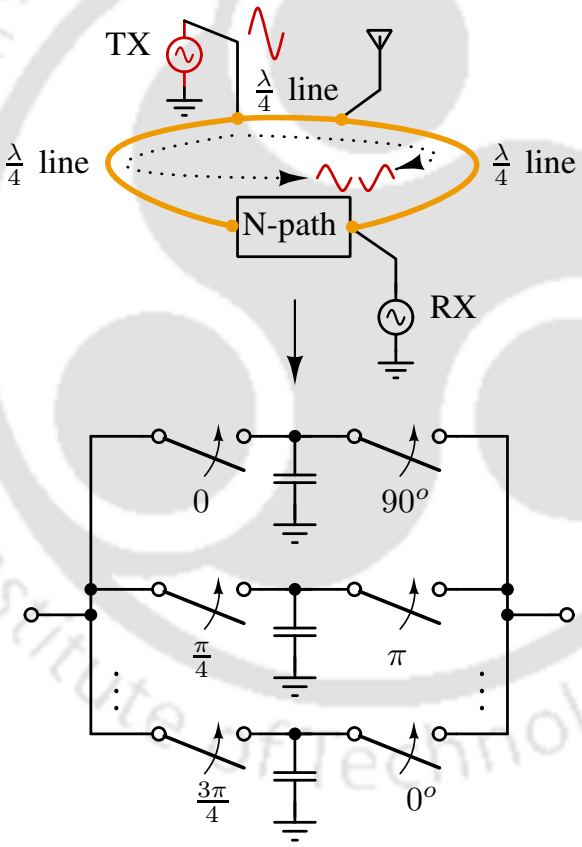


Figure 2.2: Implementation of N-path based circulator [29].

The main disadvantage of electric balanced duplexers is that there is inherit 3 dB loss. Even though the power loss can be reduced using an asymmetric duplexer topology [17]. We can not completely avoid the power loss. An alternative approach to achieve high TX-to-RX isolation is to use circulators instead of duplexers. Typically circulators require magnetic components and implemented off-chip. Recently an N-path filter based on-chip circulator was proposed in [29]. A 2-port N-path filter with

a θ degree phase shift between its two clocks provides a $+\theta$ degree phase shift in one propagation direction and -θ degree in the other, which is non-reciprocal behavior. Fig. 2.2 shows N-path based circulator [29] using a 2-port N-path filter and three $\lambda/4$ transmission lines. Each $\lambda/4$ transmission line is designed to provide $-90°$ phase shift at the RF frequency. From TX-to-RX, the signal can flow from two available paths. During the transmission, the signal flowing through two $\lambda/4$ lines undergoes a phase shift of $-180°$. Whereas on the other path, the transmitting signal undergoes $0°$ phase shift due to the non-reciprocal behavior of the N-path filter. Therefore, the signal at the receiving port cancels out. In [29], the authors demonstrate 20 dB isolation from the integrated circulator across a 12 MHz baseband bandwidth. Transmitting, receiving, and antenna ports are placed along the transmission line. The circulator is combined with analog baseband cancellation, and non-linear digital cancellation. A total of 85 dB leakage rejection is demonstrated.

2.3 Transformer based duplexer to transformer-less duplexer

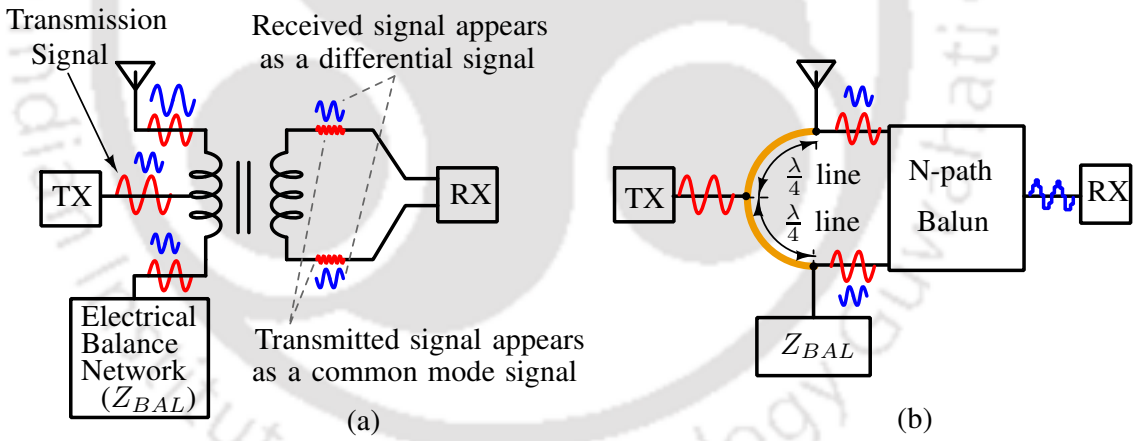


Figure 2.3: (a) A transformer-based duplexer (b) The proposed transformer-less duplexer based on N-path balun bandpass filter

Fig. 2.3(a) shows a hybrid transformer based differential duplexer with four ports: transmitter (TX) port at the center of the primary winding, antenna (ANT) port at one end of the primary winding, electrical balance (BAL) port at the other end of the primary winding, and the two terminals of the secondary winding acting as a differential receiver (RX) port. Electrical balance is a single port network designed to have the same port impedance as that of the ANT. Under the perfect balancing condition, the transmission signal that is injected into the primary winding appears with the same magnitude and phase at the two ends of the primary winding. Signals with equal magnitude-and-

phase at the ANT and BAL ports induces only a small common-mode signal at the differential RX port as shown in Fig. 2.3(a). The received signal from the antenna enters the primary winding of the transformer from one of its ends. Due to the asymmetric injection, received signal will induce a differential signal across the terminals of the secondary winding. Hence a differential receiver will process the received signal and rejects the common-mode transmitter leakage.

A transformer-less duplexer, shown in Fig. 1(b), is built based on the same port configuration and same signal processing mechanism as that of the transformer based duplexer. The proposed duplexer consists of two quarter-wavelength transmission lines and an N-path balun. Quarter-wavelength transmission lines provide -90° phase shift to the signal. The characteristic impedance of the transmission lines are optimized to achieve the input-match at the receiver port. Two quarter-wave transmission lines from the TX port will lead to two different ports: ANT and BAL. Under the perfect balancing condition, the transmission signal appears with equal magnitude and phase ($-90°$ with respect to the signal at the TX port) at the ANT and BAL ports. N-path balun, operating in differential-to-single (DS) mode, senses this common-mode signal and rejects it at its output (RX port). Similarly, a received signal enters the duplexer from the ANT port and appears as a differential input to the N-path balun. Hence the received signal is processed by the N-path balun with minimum insertion loss.

2.4 N-path BPF

Fig. 2.4(a) shows a 2-port N-path bandpass filter (BPF) consisting of 'N' identical parallel paths switching at a clock frequency of f_s. Each path consists of two switches acting as mixers and a shunt capacitor acting as a lowpass filter. The two switches in each path operate at two different clock phases separated by an angle 'θ'. Moreover, each path works at a different set of input-output clock phases as shown in Fig. 2.4(a) and Fig. 2.4(b). The operation of the 2-port N-path BPF can be explained as follows. The incoming signal is sampled by the input switches at a rate of 'N' samples per clock cycle. Each sample is lowpass filtered and held for a duration of '$\frac{\theta T_s}{2\pi}$' on the capacitor, before up-converting to the clock frequency by the output switch in each path. All the up-converted samples are combined at the output to reconstruct the original signal.

In Fig. 2.4(a), R_s is the source resistance, R_l is the load resistance, and C the capacitance in each branch. Assuming the ON-resistances of the input and output switches to be R_{sw1} and R_{sw2}

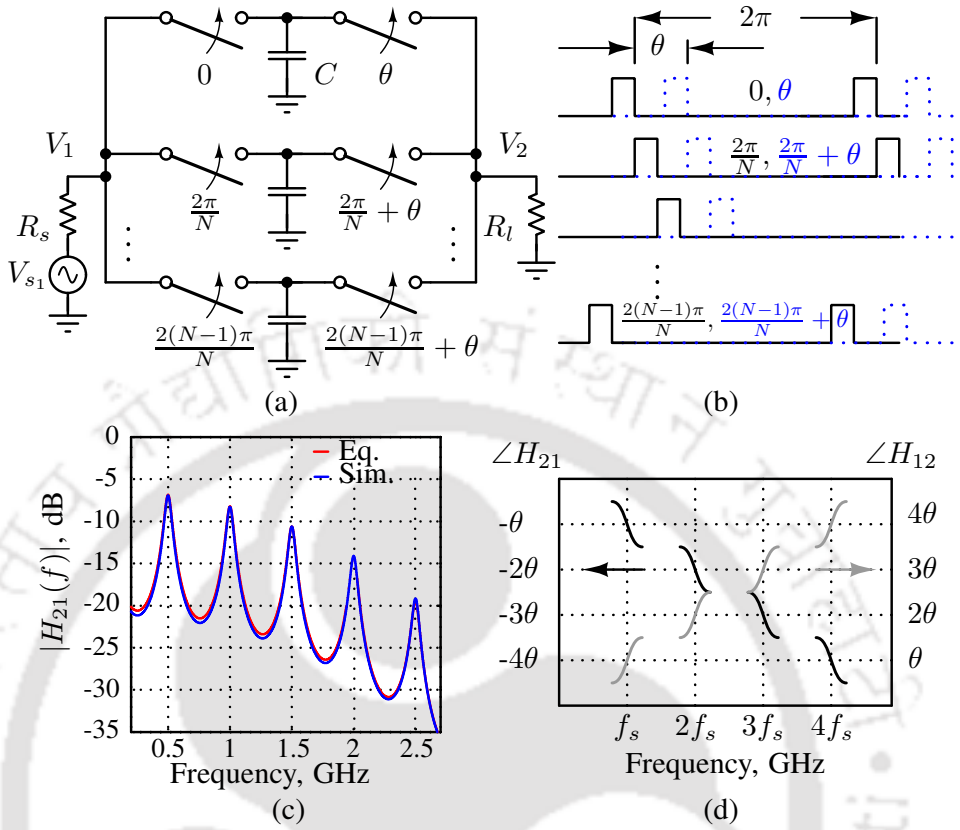


Figure 2.4: (a) A 2-port N-path BPF with different input and output clock phases. (b) Input and output clock phases (c) Magnitude response of the filter when $R_s = R_l = 50\ \Omega$, $C = 25$ pF, $R_{sw1} = R_{sw2} = 1\ \Omega$ and $f_s = 500$ MHz. (d) Phase characteristics for $\frac{2\pi}{N} \leq \theta \leq \frac{2(N-1)\pi}{N}$.

respectively, the voltage transfer function of the two port N-path BPF [26, 30] is given by

$$H_{21}(f) = \frac{V_2}{V_{s_1}} = H_0(f)\frac{R_l}{R_l + R_{sw2}} \times e^{-j\frac{f}{f_s}\theta} \tag{2.1}$$

$$\text{where } H_0(f) = \frac{N f_s e^{j\frac{f}{f_s}\frac{2(N-1)\pi}{N}}}{2\pi f_{r_lc}(1 + \frac{jf}{f_{r_sc}})(1 + \frac{jf}{f_{r_lc}})} \times \frac{(e^{\frac{j2\pi f}{Nf_s}} - e^{\frac{-2\pi f_{r_sc}}{Nf_s}})(e^{\frac{j2\pi f}{Nf_s}} - e^{\frac{-2\pi f_{r_lc}}{Nf_s}})}{e^{\frac{j2\pi f}{f_s}} - e^{\frac{-2\pi(f_{r_sc}+f_{r_lc})}{Nf_s}}}, \tag{2.2}$$

$$f_{r_sc} = \frac{1}{2\pi(R_s + R_{sw1})C}, \text{ and } f_{r_lc} = \frac{1}{2\pi(R_l + R_{sw2})C}.$$

It should be noted that the analytical expression (2.1) is valid only when the phase shift $\theta \in [\frac{2\pi}{N}, \frac{2(N-1)\pi}{N}]$. The magnitude response of an ideal 2-port N-path BPF with $R_s = R_l = 50\ \Omega$, $C = 25$ pF, $R_{sw1} = R_{sw2} = 1\ \Omega$ and $f_s = 500$ MHz is shown in Fig. 2.4(c). The analytical expression (2.1) is also plotted in Fig. 2.4(c). One can notice the magnitude peaks at all the clock harmonic frequencies. N-path filters exhibit spurious responses at the harmonics of the LO signal, which results in poor OB rejection at these harmonics. Moreover, it can be a potential problem where there is strict emission

limit. There are some recent efforts to reduce the harmonic responses in N-path filters. An RF front end with a harmonic-rejecting N-path filter is presented in [31]. It provides tunable narrow-band filtering and high attenuation at the third and fifth-order harmonics of LO signal.

At the clock frequency ($f = f_s$), assuming $R_l = R_s$, and $C \gg \frac{1}{2\pi R_s f_s}$, (2.1) can be simplified to

$$H_{21}(f_s) = H_0(f_s)\frac{R_s}{R_s + R_{sw2}}e^{-j\theta} \tag{2.3}$$

$$H_0(f_s) \approx \frac{N^2(1-\cos(\frac{2\pi}{N}))}{4\pi^2} \tag{2.4}$$

Similarly, assuming $C \gg \frac{1}{2\pi R_s f_s}$ and $R_l = R_s$, input and output impedances of the 2-port N-path BPF at $f = f_s$ can be shown to be as follows [16].

$$Z_{in}(f_s) = Z_{out}(f_s) \approx R_s \frac{N^2(1-\cos(\frac{2\pi}{N}))}{4\pi^2 - N^2(1-\cos(\frac{2\pi}{N}))} \tag{2.5}$$

Fig. 2.4(d) shows the generic phase response of the circuit shown in Fig. 2.4(a) [26]. From the $\angle H_{21}$ plot in Fig. 2.4(d), at $f = \mathrm{i} \times f_s$ for i = 1, 2, 3, ...etc., the output is phase delayed by an angle of 'i $\times \theta$' with respect to the input. Another interesting property of the 2-port N-path BPF is its phase non-reciprocity($\angle H_{21} \neq \angle H_{12}$) as shown in Fig. 2.4(d).

2.5 Proposed N-path balun BPF

A Balun BPF can be designed by connecting two 2-port N-path BPFs at the input as shown in Fig. 2.5(a). In Fig. 2.5(a), the output clocks of the upper N-path BPF are delayed by an angle of $\pi/2$ from their input clocks. From Fig. 2.4(d), $\theta = \frac{\pi}{2}$ results in an output phase shift of $-\frac{\pi}{2}$ at the fundamental frequency and $-\pi$ at the 2^{nd} harmonic frequency. Similarly, the output clocks of the lower N-path filter are delayed by an angle of $-\pi/2$ from their input clocks. This results in an output phase shift of $\frac{\pi}{2}$ at the fundamental frequency and π at the 2^{nd} harmonic frequency. The harmonic phasor diagrams of the two outputs are shown in Fig. 2.5(b). From Fig. 2.5(b), the phase difference between the two output signals is π at the fundamental frequency and 0 at the 2^{nd} harmonic frequency.

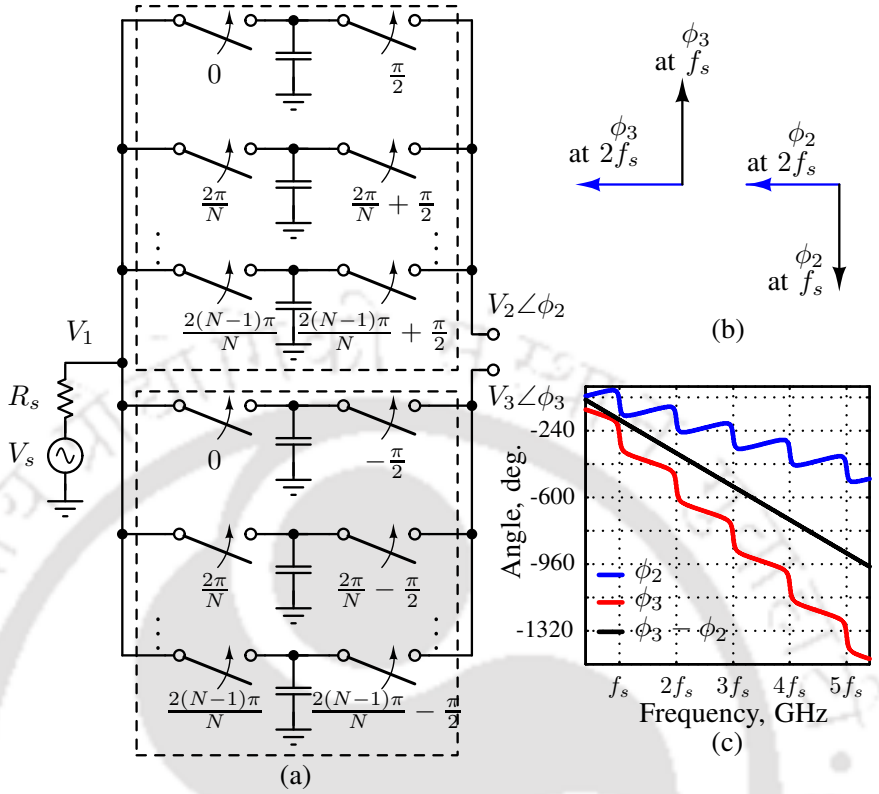


Figure 2.5: (a) Proposed Balun circuit based on two port N-path BPFs (b) Harmonic phasor diagrams of the two outputs (c) Phases of the output signals.

2.5.1 Single-to-Differential (SD) mode of operation

The differential output to single-ended input transfer function can be derived using (2.1).From Fig. 2.6(a),

$$\begin{aligned} H_{SD}(f) &= \frac{V_3 - V_2}{V_{s_1}} = \frac{V_3 - V_2}{V_1}\frac{Z_{in}}{Z_{in}+2R_s} \\ &= H_0(f)\frac{R_l}{R_l+R_{sw2}}\frac{Z_{in}+R_s}{Z_{in}}(e^{j\frac{f}{f_s}\frac{\pi}{2}} - e^{-j\frac{f}{f_s}\frac{\pi}{2}})\frac{Z_{in}}{Z_{in}+2R_s} \\ &= H_0(f)\frac{R_l}{R_l+R_{sw2}}\frac{Z_{in}+R_s}{Z_{in}+2R_s} \times 2j\sin(\frac{f}{f_s}\frac{\pi}{2}) \\ &= \begin{cases} 0 & \text{for even harm.} \\ H_0(f)\frac{2jR_l}{R_l+R_{sw2}}\frac{Z_{in}+R_s}{Z_{in}+2R_s} & \text{for odd harm.} \end{cases} \end{aligned} \tag{2.6}$$

where Z_{in} refers to the input impedance of a single 2-port N-path BPF.

At the clock frequency ($f = f_s$), under the assumptions of $R_l = R_s$ and $C \gg \frac{1}{2\pi R_s f_s}$, (2.6) can be

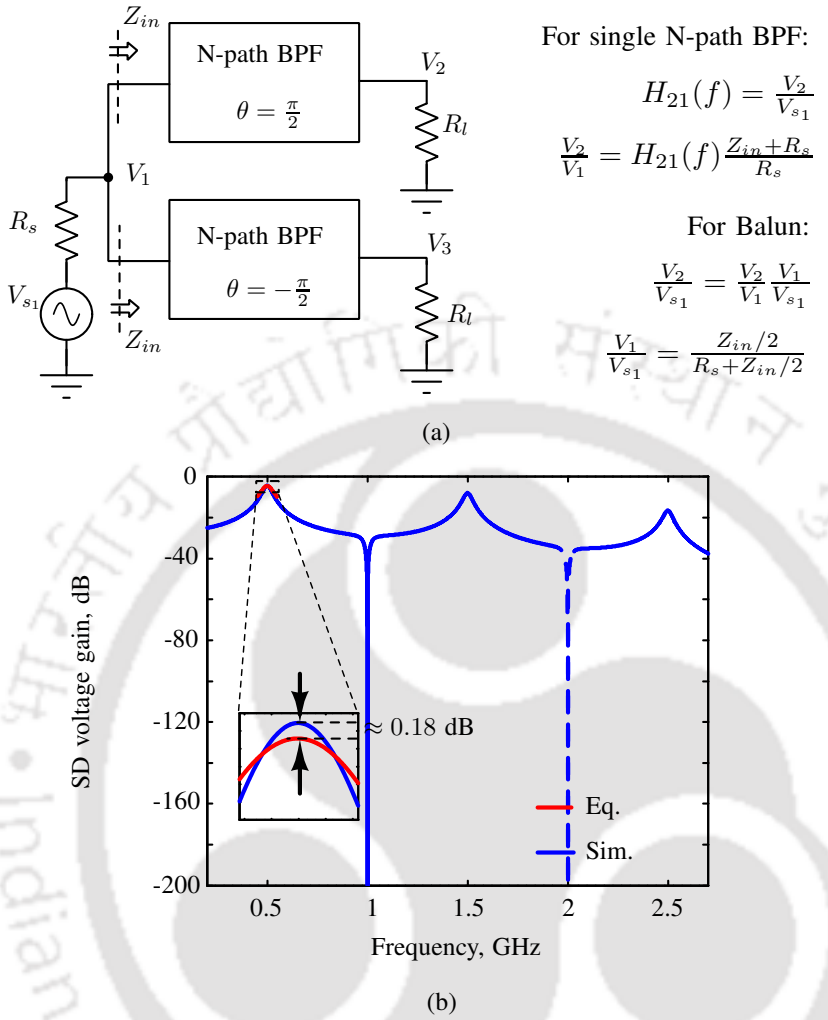


Figure 2.6: (a) Computation of Single-to-Differential (SD) voltage gain in the Balun BPF. (b) Simulated SD voltage gain of the Balun.

reduced to (2.7) using (2.5).

$$H_{SD}(f_s) \approx \frac{2jR_s}{R_s + R_{sw2}} \times \frac{N^2(1-\cos(\frac{2\pi}{N}))}{8\pi^2 - N^2(1-\cos(\frac{2\pi}{N}))} \tag{2.7}$$

The analytical expression in (2.7) has been validated by the design and simulation of a Balun using ideal elements. The design uses 50 pF capacitors and 2 Ω switches. Fig. 2.6(b) shows the simulated SD transfer functions of the Balun overlapped with the corresponding analytical expression. As shown in Fig. 2.6(b), the difference between the estimated in-band SD voltage gain and the simulated voltage gain is < 0.2 dB.

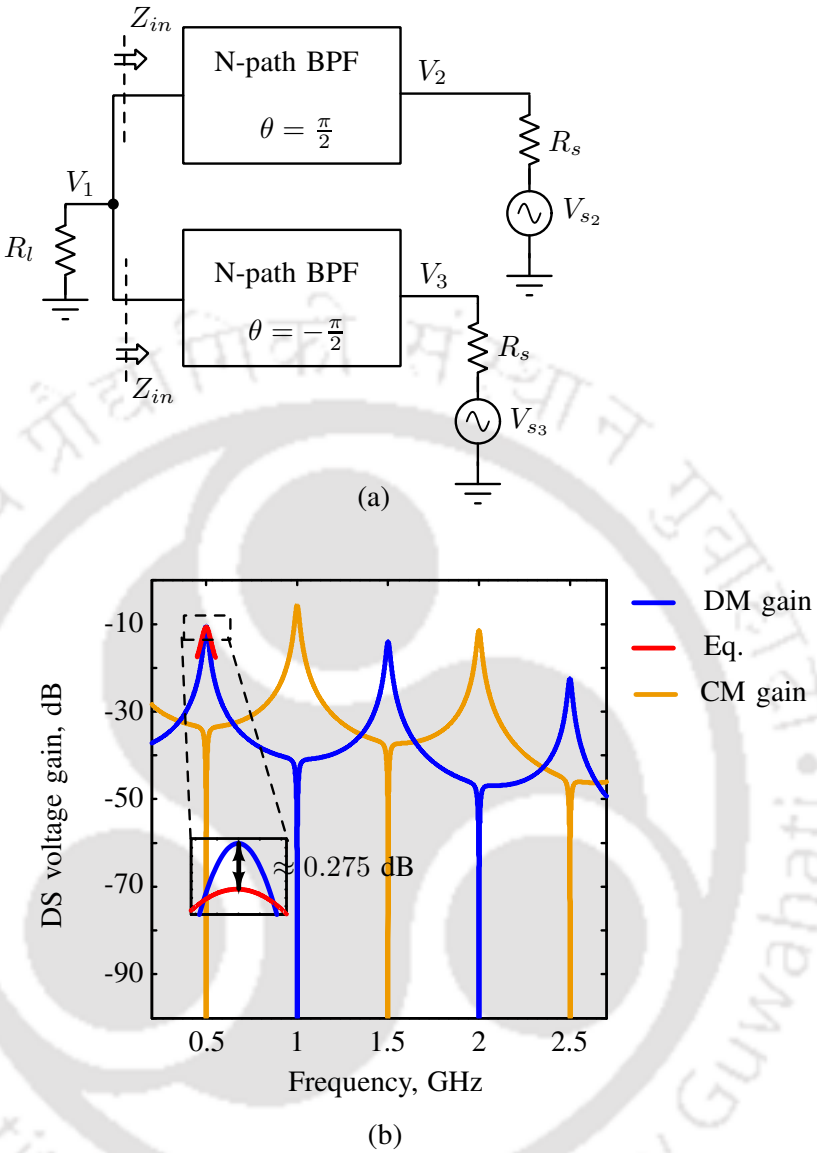


Figure 2.7: (a) Computation of Differential-to-Single (DS) voltage gain of the Balun BPF. (b) Simulated DS voltage gain of the Balun.

2.5.2 Differential-to-Single (DS) mode of operation

The Balun in Fig. 2.5(a) can also be used in the reverse direction as shown in Fig. 2.7(a), to convert a differential signal between the ports 2-and-3 to a single ended signal at port 1. The differential to

single-ended voltage gain in Fig. 2.7(a) can be derived as

$$\begin{aligned} H_{DS}(f) &= \frac{V_1}{V_{s_2} - V_{s_3}} = \frac{H_{12}V_{s_2} + H_{13}V_{s_3}}{V_{s_2} - V_{s_3}} \\ &= H_0(f)\frac{R_l'}{R_l' + R_{sw2}} \times \frac{e^{j\frac{f}{f_s}\frac{\pi}{2}}V_{s_2} + e^{-j\frac{f}{f_s}\frac{\pi}{2}}V_{s_3}}{V_{s_2} - V_{s_3}} \\ &= \begin{cases} H_0(f)\frac{R_l'}{R_l'+R_{sw2}} \times \frac{V_{s_2}+V_{s_3}}{V_{s_2}-V_{s_3}} & \text{for} \quad \text{even harm.} \\ H_0(f)\frac{R_l'}{R_l'+R_{sw2}} \times j & \text{for} \quad \text{odd harm.} \end{cases} \end{aligned} \tag{2.8}$$

where $R_l' = \frac{R_l Z_{in}}{R_l + Z_{in}}$ should be used in place of R_l. For a differential input, $V_{s_3} = -V_{s_2}$ and (2.8) reduces to zero for all even harmonics. At the clock frequency ($f = f_s$), under the assumption of $C \gg \frac{1}{2\pi R_s f_s}$, (2.8) can be reduced to (2.9) using (2.5)

$$H_{DS}(f_s) \approx H_0(f_s)\frac{N^2(1-\cos(\frac{2\pi}{N}))R_s}{N^2(1-\cos(\frac{2\pi}{N}))R_s + 4\pi^2 R_{sw2}} \times j \tag{2.9}$$

where $H_0(f_s)$ should be computed from (2.2).

Similarly, the common-mode voltage gain is given by

$$\begin{aligned} H_{CM}(f) &= \frac{V_1}{\frac{V_{s_2}+V_{s_3}}{2}} = \frac{2(H_{12}V_{s_2} + H_{13}V_{s_3})}{V_{s_2} + V_{s_3}} \\ &= 2H_0(f)\frac{R_l'}{R_l' + R_{sw2}} \times \frac{e^{j\frac{f}{f_s}\frac{\pi}{2}}V_{s_2} + e^{-j\frac{f}{f_s}\frac{\pi}{2}}V_{s_3}}{V_{s_2} + V_{s_3}} \\ &= \begin{cases} 2H_0(f)\frac{R_l'}{R_l'+R_{sw2}} & \text{for} \quad \text{even harm.} \\ 2H_0(f)\frac{R_l'}{R_l'+R_{sw2}} \times \frac{j(V_{s_2}-V_{s_3})}{V_{s_2}+V_{s_3}} & \text{for} \quad \text{odd harm.} \end{cases} \end{aligned} \tag{2.10}$$

For a common-mode input, $V_{s_3} = V_{s_2}$ and (2.10) reduces to zero for all odd harmonics. The analytical expression in (2.9) has been validated by the design and simulation of a Balun using ideal elements. The design uses 50 pF capacitors and 2 Ω switches. Fig. 2.7(b) shows the simulated transfer function of the Balun overlapped with the corresponding analytical expression. As shown in Fig. 2.7(b), the difference between the estimated in-band voltage gain and the simulated voltage gain is < 0.3 dB.

2.5.3 Simulation results

The proposed Balun is implemented in CMOS 65 nm LL technology and occupies an active area of ≈ 0.7 mm^2. A layout image of the implemented Balun is shown in Fig. 2.8(a). The switches of the Balun are implemented by NMOS transistors and are sized to have an ON-resistance of 2 Ω each. MIM capacitors are used to implement the 50 pF capacitors. The phase difference between the output

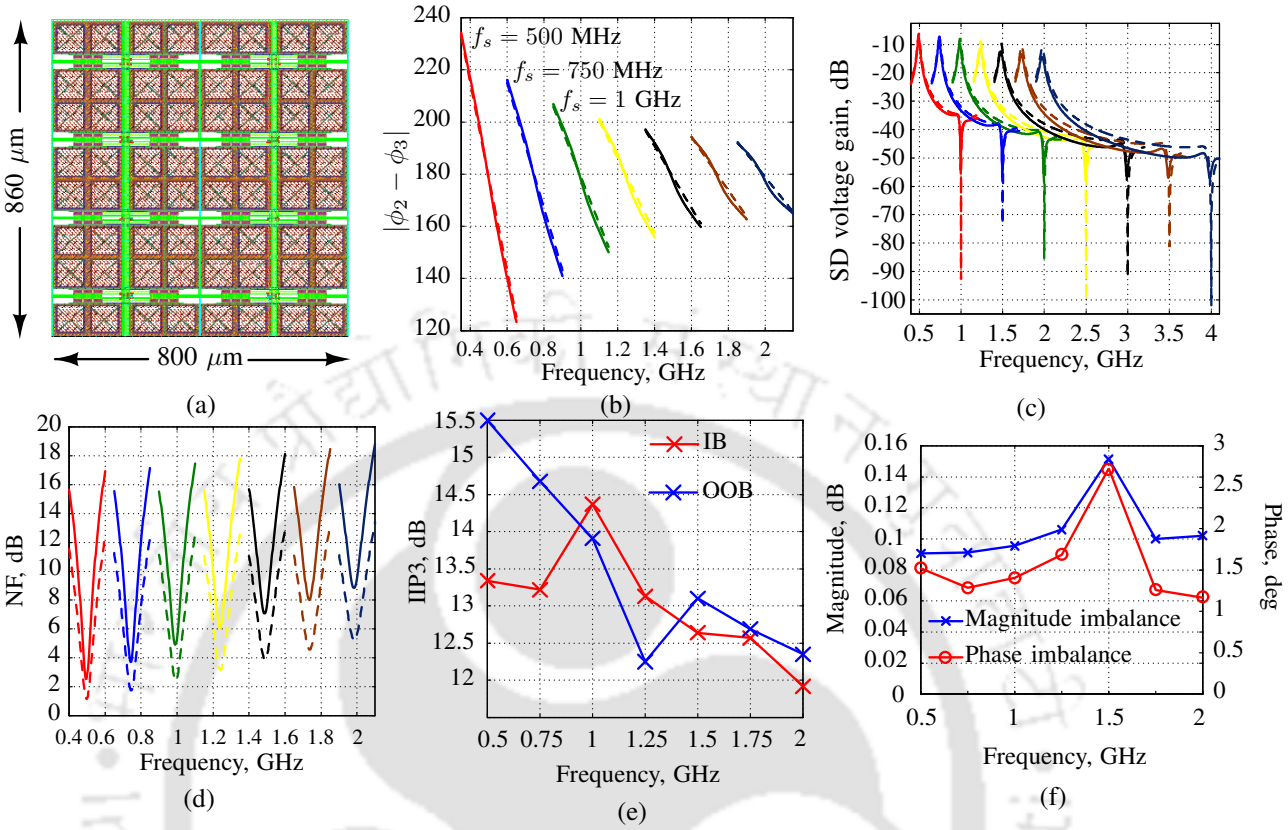


Figure 2.8: (a) Layout of the Balun in CMOS 65 nm technology. Schematic (−−) and post-layout (—) results: (b) Phase difference between the outputs at different clock frequencies, (c) SD magnitude response of the Balun, (d) SD Noise figure (NF), (e) SD In-band and out-of-band IIP3, (f) Amplitude and phase imbalances between the outputs during the SD operation.

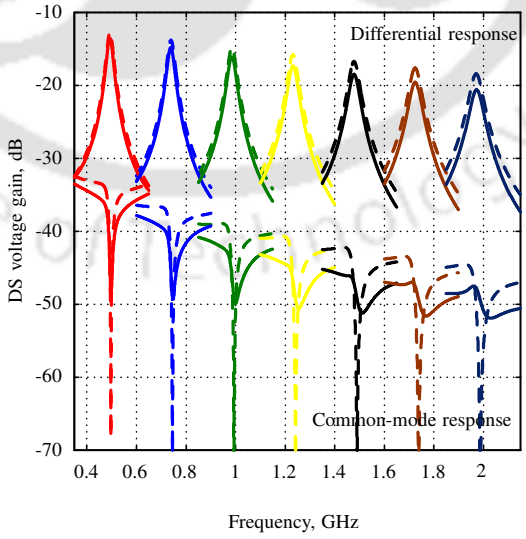


Figure 2.9: Common-mode and differential responses during the DS operation. Dashed lines are schematic results and solid lines are post-layout results.

ports (2-and-3) in SD operation is shown in Fig. 2.8(b) and is ≈ 180° at every clock frequency. The SD voltage transfer function is shown in Fig. 2.8(c) at different clock frequencies. In Fig. 2.8(c), one can observe a notch at every second harmonic frequency. The NF of the Balun during SD operation is shown in Fig. 2.8(d). The IB-IIP3 and OB-IIP3 are shown in Fig. 2.8(e). The two tones are separated by 5 MHz in IB-IIP3 simulation and 30 MHz in OB-IIP3 simulation. Amplitude and phase imbalances are two important parameters of interest in the case of a Balun. Phase imbalance is the deviation of the phase difference between the outputs from 180° and amplitude imbalance is the difference in magnitudes of the two outputs. Fig. 2.8(f) shows the amplitude and phase imbalances between the outputs during the SD operation. The differential and common-mode voltage gains (output at port 1) during the DS operation are shown in Fig. 2.9. One can observe a notch at every clock frequency in the common-mode response, in Fig. 2.9, indicating common-mode rejection. The bandwidth of the Balun is 22 MHz. The performance of the Balun is summarized in Table. 2.1.

Table 2.1: Performance Summary of the Balun Over the Tuning Range of 0.1-to-1 GHz

	Schematic	Post-layout
IB SD voltage gain† (dB)	-5.2 to -8.1	-5.6 to -9.9
IB DS voltage gain† (dB)	-11.3 to -14.8	-11.7 to -16.6
IB common-mode voltage gain† (dB)	-54.8 to -80.4	-48.3 to -49.9
SD NF (dB)	0.6-2.4	1.3-4.9
SD IB IIP3‡ (dBm)	12.6 to 18.8	12.1 to 14.4
SD OB IIP3‡ (dBm)	13.9 to 20.7	13.3 to 15.6
Amplitude imbalance (dB)	< 0.05	< 0.2
Phase imbalance* (°)	< 2	< 2.5
Bandwidth (MHz)	22	
Area (mm^2)	0.7	

† including the 50 Ω source resistance(s)
‡ f_1=f_{LO}-1 MHz and f_2=f_{LO}-6 MHz are used for IB-IIP3. f_1=f_{LO}-30 MHz and f_2=f_{LO}-59 MHz are used for OB-IIP3

The proposed Balun can be used in different applications due to its on chip implementation. It has inherent property of impedance transformation.The ratio of secondary to primary impedance is 2:1.It is used in electrical balance based duplexers which provides good TX-to-RX isolation.

2.6 Analysis of the proposed duplexer

In the following analysis, perfect balancing between the ANT and BAL ports is assumed. Also N-path filters are assumed to be ideal.

2.6.1 During the Transmitting Mode

From section 2.4, the input impedance and magnitude transfer function of a 2-port N-path BPF are independent of the embedded phase shift (θ). The symmetry, at TX port, causes the transmission signal in the proposed duplexer to split equally between the ANT and BAL ports. In other words, the transmission signal appears as a common-mode signal to the N-path balun and hence the RX port acts as a short circuit for the transmission signal. A half equivalent circuit of the balun, during the transmission mode, can be constructed as shown in Fig. 2.10(b). Due to the transparent nature of

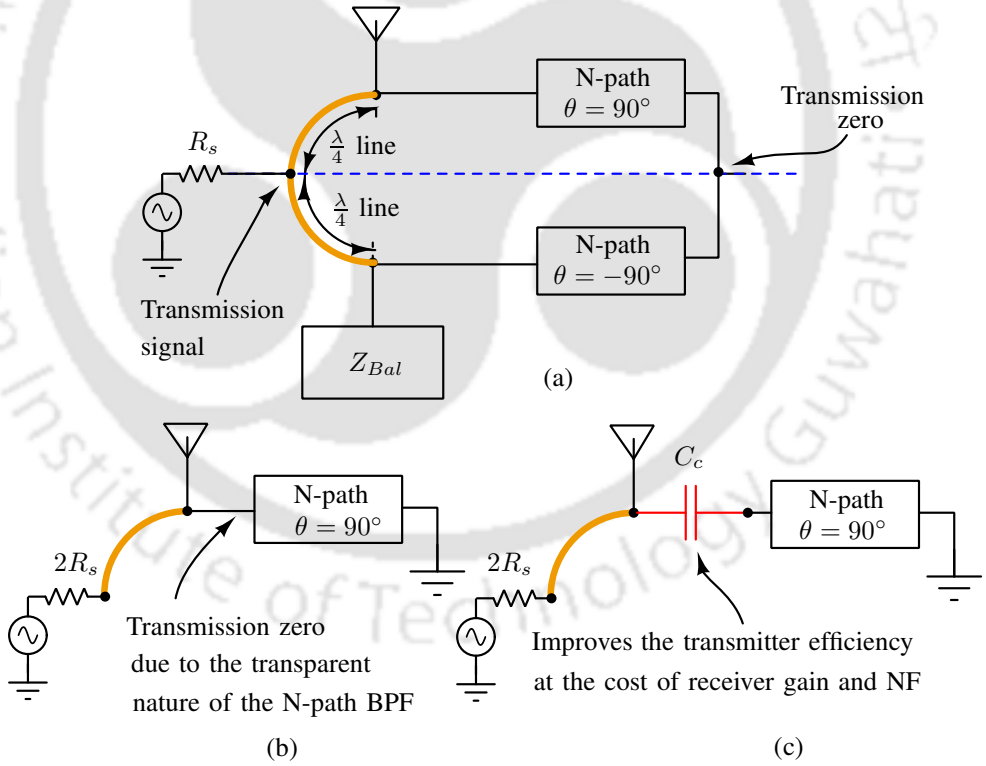


Figure 2.10: (a) Duplexer and (b) its half equivalent circuit during the transmission mode. (c) Introduction of a series capacitor to improve the transmission efficiency.

N-path BPF, the input impedance of a 2-port N-path filter with short-circuited output port is very low (depends on the switch resistances). Hence a majority of the transmitted signal flows into the balun rather than flowing out of the antenna port. Adding a suitably valued series capacitor in front

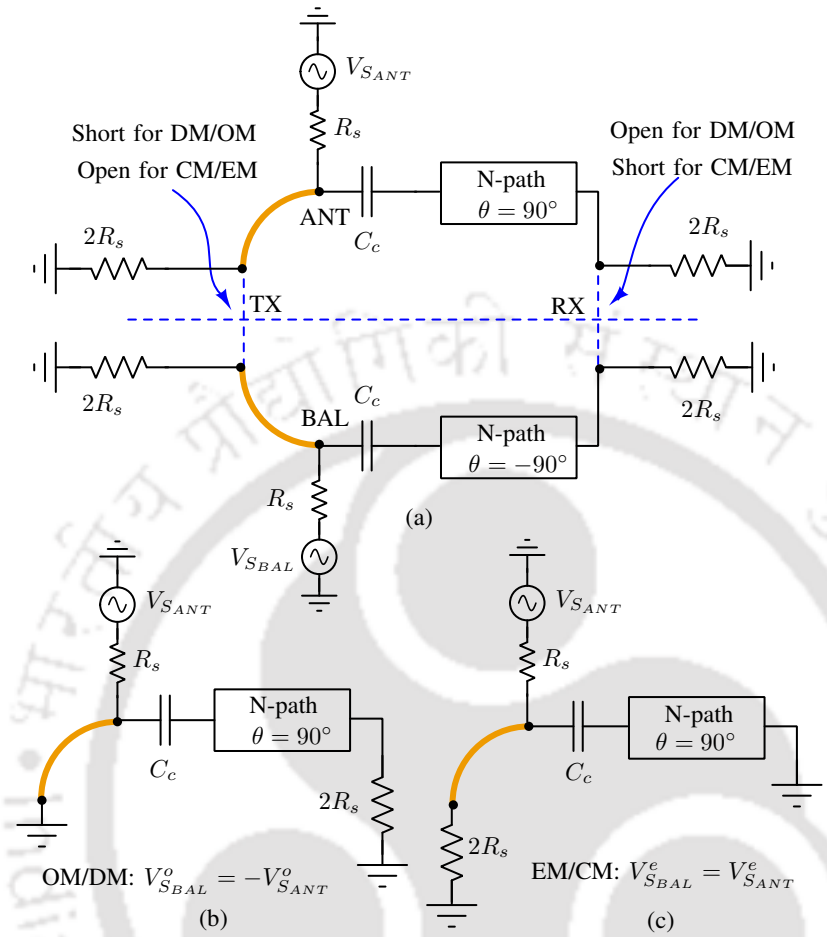


Figure 2.11: (a) Proposed duplexer during the receiving mode. Equivalent half circuits for (b) odd-mode excitation and (c) even mode excitation.

of the balun branch, as shown in Fig. 2.10(c), can increase the input impedance looking into the balun and improves the TX-to-ANT efficiency. One disadvantage of the series coupling capacitor is that it reduces the ANT-RX gain. The TX-to-ANT insertion loss (IL) can be derived as

$$S_{TX-ANT} = -j\frac{2Z_l Z_0}{Z_0^2 + 2R_s Z_l} \tag{2.11}$$

where Z_0 is the characteristic impedance of the transmission line, R_s is the TX (and RX) port impedance, Z_l is total impedance ($R_s \parallel (\frac{1}{j\omega C_c} + Z_{Npath})$) at the ANT port, C_c is the coupling capacitor and Z_{Npath} is the input impedance of the N-path BPF with short-circuited output.

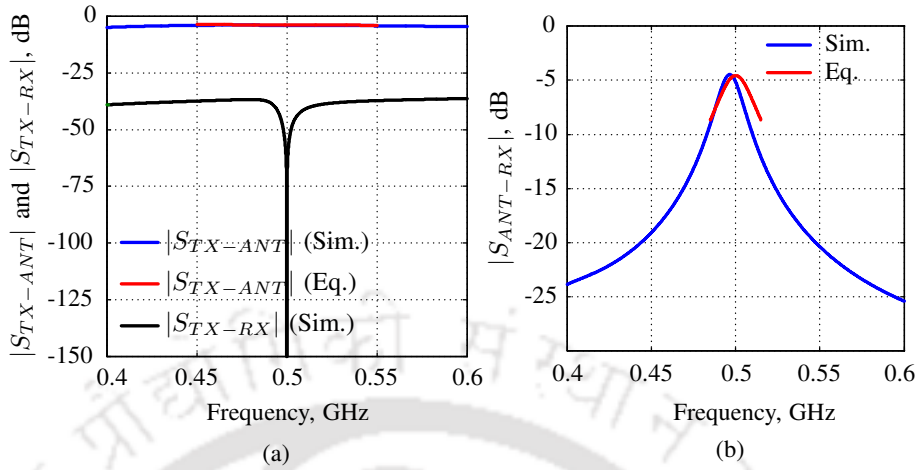


Figure 2.12: (a) Transmitter to antenna loss and transmitter to receiver isolation of the proposed duplexer. (b) Antenna to receiver insertion loss.

2.6.2 During the Receiving Mode

Even-and-odd mode analysis can be used to study the operation of the duplexer during the receiving mode. During the odd-mode (OM) excitation, a differential signal ($V^o_{S_{BAL}} = -V^o_{S_{ANT}}$) is applied across the ANT and BAL ports. OM excitation causes a null at the TX port. The equivalent half circuit of the duplexer for OM is shown in Fig. 2.11(b). During the even-mode (EM) excitation a common-mode signal ($V^e_{S_{BAL}} = V^e_{S_{ANT}}$) is applied across the ANT and BAL ports. EM causes a null at the RX port. Fig. 2.11(c) shows the equivalent half circuit of the duplexer during the EM excitation. The ANT to RX insertion loss is given by

$$\begin{aligned} S_{ANT-RX} &= 2\frac{V^e_{RX} + V^o_{RX}}{V^e_{S_{ANT}} + V^o_{S_{ANT}}} = \frac{0 + V^o_{RX}}{V_{S_{ANT}}} \\ &= \frac{V^o_{RX}}{V_{ANT}} \frac{V_{ANT}}{V_{S_{ANT}}} \\ &= H_{21}(f) \frac{Z_{in} + R_s}{Z_{in}} \frac{Z_{in}}{Z_{in} + R_s + \frac{1}{\omega C_c}} \\ &= H_{21}(f) \frac{Z_{in} + R_s}{Z_{in} + R_s + \frac{1}{j\omega C_c}} \end{aligned} \tag{2.12}$$

where $V_{S_{ANT}}$ is the source voltage at the antenna port, R_s is the port impedance of all ports, Z_{in} is the input impedance of the N-path BPF, and $H_{21}(f)$ is the voltage transfer function of the N-path BPF including a source resistance R_s.

The analytical expressions (2.11) and (2.12) are validated by the design and simulation of a duplexer

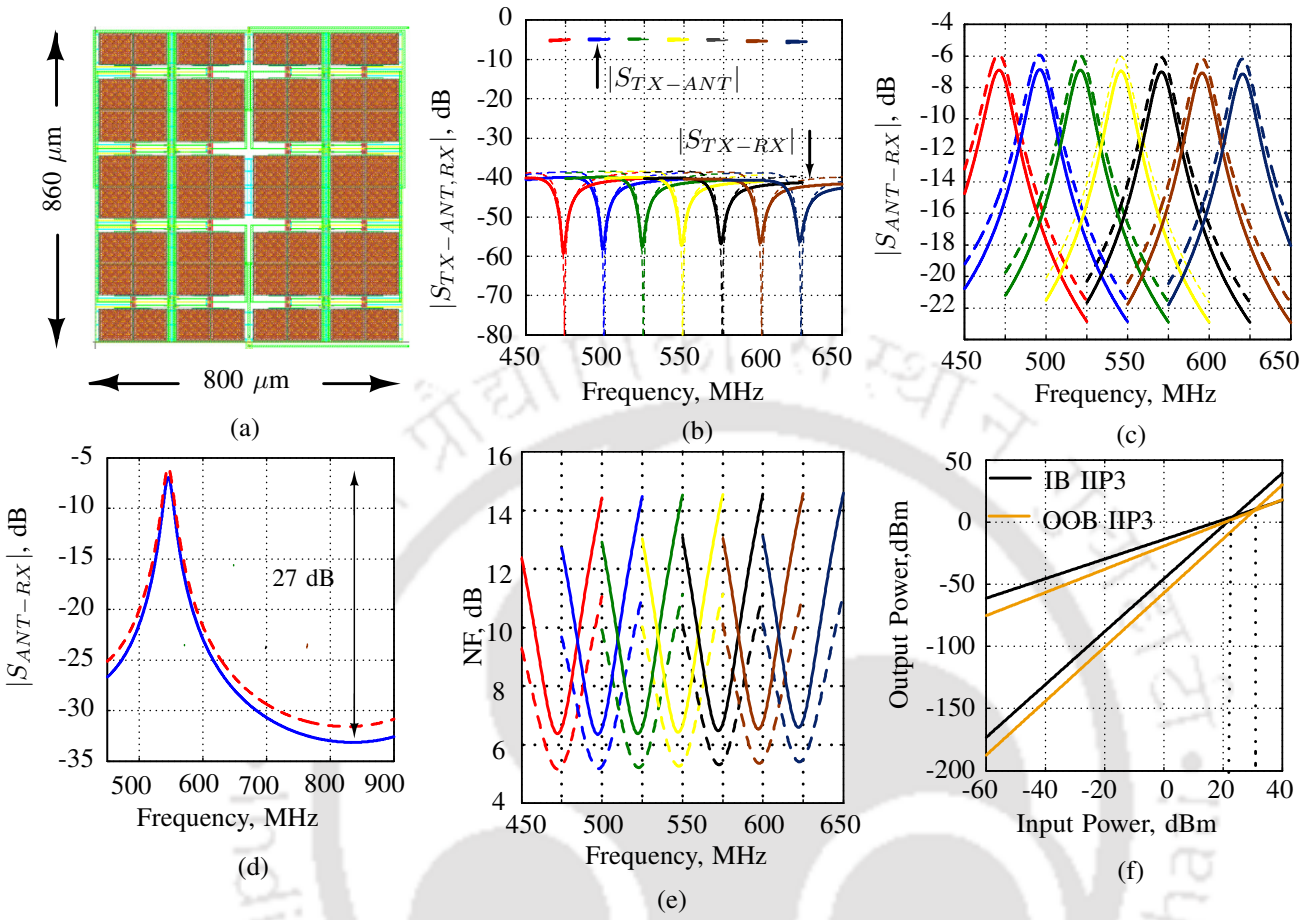


Figure 2.13: (a) An image of the duplexer layout. Schematic (−−) and post-layout (—) results of the duplexer: (b) TX-ANT insertion loss and TX-to-RX isolation (c) ANT-RX insertion loss (d) OB filtering during the receiving mode (e) NF during the receiving mode (f) IB-IIP3 and OB-IIP3 during the receiving mode. (The simulated IB-IIP3 is 20 dBm with f_1=549 MHz and f_2=544 MHz. The simulated OB-IIP3 is 29 dBm with f_1=495 MHz and f_2=441 MHz.)

with ideal components. In simulations, quarter-wave transmission lines are replaced by their equivalent lumped models. N-path filters are implemented using 50 pF capacitors and ideal switches. Eight paths are used in the filter. Fig. 2.12(a) shows the TX-to-RX isolation and TX-to-ANT loss. Analytical expression (2.11) is also plotted in Fig. 2.12(a). Fig. 2.12(b) shows the simulated and computed (from (2.12)) ANT-to-RX loss.

2.7 CMOS implementation and simulations

A prototype duplexer has been implemented with an on-chip balun in 65 nm CMOS technology and off-chip lumped element quarter-wave lines. N-path filters in the balun use 50 pF MIM capacitors

Table 2.2: Performance Comparison of the Duplexer

Parameter	[17]	[18]	[19]	[32]	[33]	This work†
Architecture	Transformer	Transformer	Transformer	N-path coupler	Baseband duplexing	N-path Balun
FDD/SC-FD	FDD	FDD	FDD	SC-FDD	FDD	FDD & SC-FD
RX Type	Differential	Differential	Differential	Single-ended	Single-ended	Single-ended
TX-RX Isolation (dB)	$>$ 45	$>$ 50	$>$ 50	40	30	$>$ 55
TX-ANT IL (dB)	2.5	$<$ 3.7	4.5	3.1	NA	5
ANT-RX IL (dB)	NA	$<$ 3.9	$<$ 3 *	NA	0	7
OB Rejection (dB)	NA	NA	NA	NA	NA	27
N.F (dB)	5	NA	6.7‡	2.7	5.5	$<$ 7
ANT-RX IIP3 (dBm)	NA	72	$<$ 0 *	-4	-38	20
Freq. (GHz)	1.5-2.4 *	1.9-2.2	1.7-2.2 *	0.55-0.9	0.1-1.5	0.45-0.65
Tech (nm)	65	180	65	65	65	65
Area (mm^2)	0.2	1.75	2.2	NA	1.5	0.7

† Post layout results (the results can degrade in measurements); * Estimated from plots; ‡ Cascaded NF

and NMOS switches with 6 Ω of ON-resistance. Eight paths are used in the filter. A layout image of the balun is shown in Fig. 2.13(a). The characteristic impedance of the off-chip lumped element transmission line is ≈70.7 Ω. The coupling capacitors C_c have a value of 6 pF. Fig. 2.13(b) shows the TX-to-ANT insertion loss and TX-to-RX isolation. ANT-to-RX gain is shown in Fig. 2.13(c). The duplexer has an ultimate rejection of ≈27 dB, as shown in Fig. 2.13(d), during the receiving mode. The ANT-to-RX path of the duplexer is (clock) tunable from 450 MHz to 650 MHz without tuning (or changing the LC values) the transmission lines. The duplexer has a NF $<$ 7 dB over the tuning range of 450 MHz to 650 MHz. NF plots are shown in Fig. 2.13(e). IIP3 of the duplexer during the receiving mode is shown in Fig. 2.13(f). In the graphs of Fig. 2.13, solid lines represent the post-layout results and dashed lines represent the schematic results. Due to the parasitic resistance in each path of the balun, the ANT-RX insertion loss and hence NF are degraded in post-layout simulations. Even though the layout is drawn to be symmetrical, there are mismatches in the clock path of the upper and the lower N-path filter. These mismatches cause offset in the output phases of the two N-path filters. Therefore, in the post-layout simulations, TX-to-RX isolation is degraded. The performance of the proposed duplexer is summarized and compared with the existing literature in Tab. 2.2. It can be seen that TX-to-ANT insertion loss limits the RX NF. The proposed duplexer provides frequency tunability and out-of-band rejection but TX-to-ANT insertion loss is poorer than

transformer based duplexers [18]. The inherit 3 dB TX-to-ANT insertion loss can be reduced by introducing the asymmetry in the balanced duplexers. [17] reports 2.5 dB TX-to-ANT insertion loss using asymmetrical balanced duplexer.

The main disadvantage of N-path filters or N-path mixer first receivers is the leakage of clock signal to the antenna port. Typical clock leakage in the N-path circuits is in order of -60 dBm. There are some recent efforts to reduce the clock leakage in N-path circuits [34]. Using the technique proposed in [34], the clock leakage can be reduced by another 15 dB.

3

Transmitter Echo Cancellation

Contents

3.1 Introduction

IB FD radios, which can simultaneously transmit and receive at the same frequency, offer twice the throughput in comparison to the traditional FDD systems. One major problem that prevents the usability of an FD radio in practice is the self-interference (SI) [3] caused by the leakage and echo signals from the transmitter (TX) to its own receiver (RX). In an FD radio, the transmitter leakage is caused by the on-chip or on-board parasitic paths between the transmitter and the receiver. A transmitter echo is an attenuated, delayed and phase-shifted version of the transmitted signal which enters the receiver from free space. In a two antenna system, the transmitter leakage is usually very low at radio frequencies but could be very high at millimeter-wave (mm-wave) frequencies due to the proximity of the TX and RX antennas. In a single antenna system, transmitter leakage can be reduced by using an electrical balanced duplexer (EBD) [4–8] or a circulator [9–11]. [32, 35] present laboratory demonstrations of single-antenna interface circuits (over a wired test setup) with $>$ 40 dB transmitter leakage reduction. [36] demonstrates the transmitter leakage cancellation exploiting the SI reflection [37] demonstrates on-board implementation of a tunable FDD system.

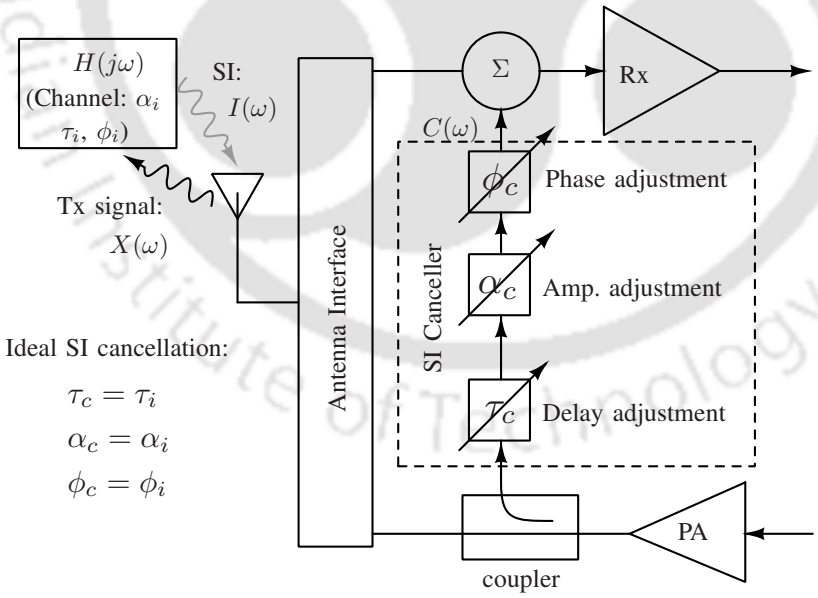


Figure 3.1: Block diagram of a typical FD transceiver including an SI canceller. The canceller path should provide the amplitude, phase, and group delay tunability.

Transmitter echo cancellation requires an SI canceling signal. Fig. 3.1 shows a typical full-duplex receiver. From Fig. 3.1, if a transmitted signal $X(\omega)$ experiences an attenuation α_i, a time delay τ_i and a phase delay ϕ_i before becoming an echo then the near-by channel can be modeled to have

a transfer function of $H(j\omega) = \alpha_i e^{-j\omega_i\tau_i + j\phi_i}$. The SI caused by the transmitter echo is given by $I(\omega) = \alpha_i e^{-j\omega_i\tau_i + j\phi_i} X(\omega)$. One way to mitigate the problem of SI is to create an SI canceling signal which when combined with the received signal will nullify the SI present in it. A canceller signal $C(\omega)$ can be generated by tapping a copy of the TX signal $X(\omega)$ and adjusting its amplitude, delay, and phase. Therefore the SI-canceling circuit that generates the canceller signal $C(\omega)$ should be capable of providing a variable attenuation α_c, a variable time delay τ_c and a variable phase delay ϕ_c. To cancel the SI completely, one needs to set $\alpha_c = \alpha_i$, $\tau_c = \tau_i$ and $\phi_c = \phi_i$. Any mismatch in amplitude, delay or phase will result in an incomplete cancellation of the SI. If the canceller signal has only a phase mismatch $\Delta\phi$ then the residual SI in the receiver is given by $I(\omega) - C(\omega) = (1 - e^{j\Delta\phi})I(\omega)$. The magnitude of SI cancellation (SIC) is given by $SIC = \sqrt{2 - 2cos\Delta\phi}$. Fig. 3.2 shows the variation of SIC with phase mismatch. From Fig. 3.2, an SI canceler with higher phase resolution offers better SIC.

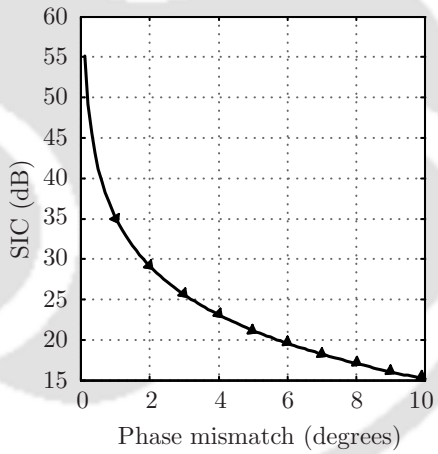


Figure 3.2: Effect of phase mismatch between the SI and the canceller signals on SIC.

Many on-chip SI-canceling circuits have been proposed in the recent past. [13] presents a passive SI-canceling circuit based on a vector modulator (VM) downmixer. The VM presented in [13] is discrete in nature, i.e., the VM constellation consists of a few discrete points. In general, a large number of VM slices (31-slices are used in [13]) are needed to cover a sufficient number of constellation points. Moreover, the NF of the receiver in [13] degrades by more than 4 dB in FD mode. The FD receiver presented in [13] can tolerate a maximum TX power of 1.5 dBm and achieves a worst-case SIC of 15.6 dB at a group delay of 4 ns. [12] presents an SI cancellation scheme based on frequency-domain equalization at RF using $G_m - C$ N-path bandpass filters. The SI canceller filters used in [12] occupy a

large chip area mainly due to the number of capacitor banks but achieves a good SIC over a large group delay of 24 ns. [14,15] present two-point active SI-cancellation scheme based on RF and baseband (BB) adaptive filters. The frequency range of the FD receiver in [14] is limited to 0.5 GHz (1.7-2.2 GHz) due to the limited tunability of the adaptive filters.

This work presents a frequency-agile IB-FD receiver with an SI-canceling scheme based on a passive continuous-mode charge-sharing VM downmixer. Covering continuous regions on VM-constellation, low NF degradation during the FD mode, frequency agility and high effective IIP3 are some of the key features of the proposed SI-canceling circuit.

The rest of the chapter is organized as follows. Section 3.2 reviews the transmitter echo canceling circuits for FD receivers. Section 3.3 describes the architecture of the FD receiver. Section 3.4 provides the analysis of the receiver. CMOS implementation details and measurement results are presented in Section Section 3.5 and Section 3.6 respectively.

3.2 Review of transmitter echo canceling circuits

In this section, we will review various echo canceling techniques [12–14] in the FD system.

3.2.1 N-path $G_m - C$ canceller filter [12]

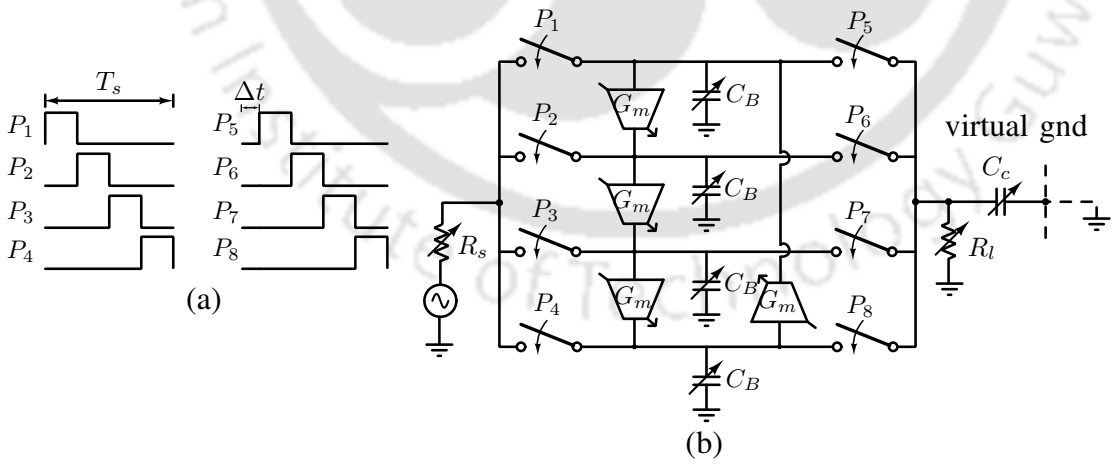


Figure 3.3: Implementation of the $G_m - C$ based N-path canceller filter [12].

2-port N-path filter has emerged in recent years due to its high Q bandpass filtering characteristics. It has N identical parallel paths. Each path consists of a capacitor and two switches operating at two different non-overlap clock signals. It has a unique property of embedded phase shifting, which is

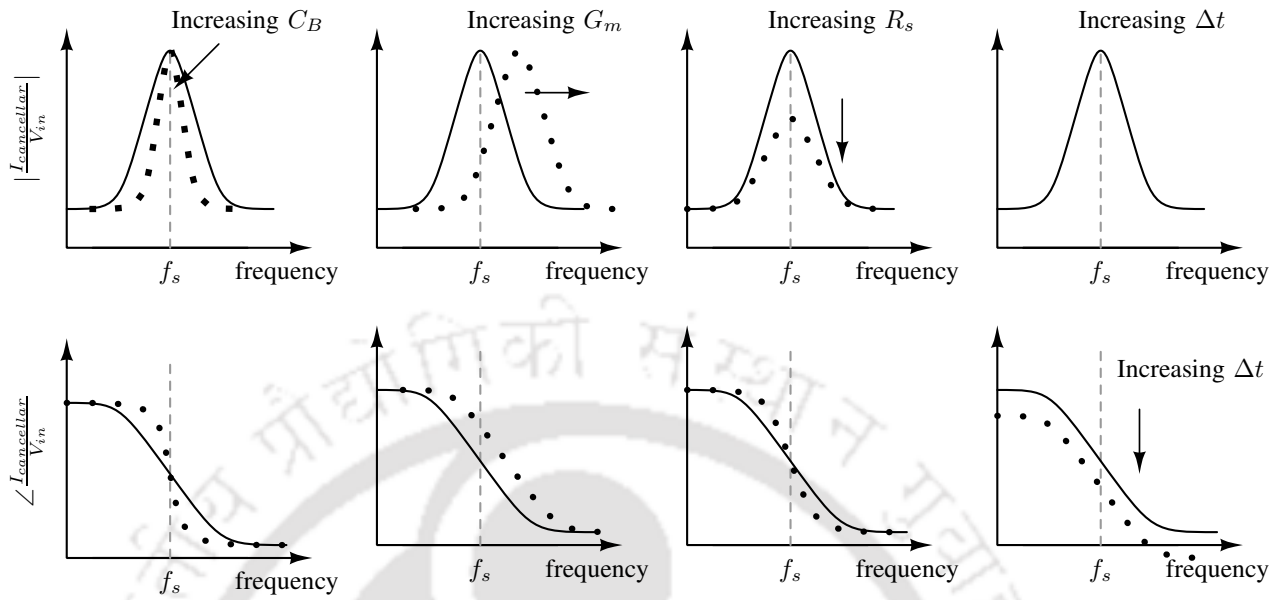


Figure 3.4: Magnitude and phase response of N path $G_m - C$ canceller filter [12].

controlled by the separation between two clock signals. The functionality and characteristics of a 2-port N-path filter are described in [38]. In [12], a $G_m - C$ based N-path filter is proposed, which has amplitude as well as phase tunning. Fig. 3.3 shows the implantation of the N path $G_m - C$ canceler filter where R_s and R_l are resistive loads at the transmitter and receiver, respectively. The capacitor C_C couples the cancellation signal $I_{canceller}$ to the receiver for SI cancellation. Two sets of non-overlapping clocks of time period, T_s separated by Δt time are used to operate it, as shown in Fig. 3.3. The Quality factor of the filter can be controlled by tunning capacitor C_B. The Quality factor changes the bandwidth of the filter, as shown in Fig. 3.4. The expression of Quality factor is derived in [39]

$$Q = 4\pi f_s[(R_s + R_{on})||(R_l + R_{on})]C_B \tag{3.1}$$

where R_{on} is switch on-resistance and f_s is the clock frequency. Under SI cancellation, the output node is at the virtual ground, and the current $I_{canceller}$ flows into the ground. The transfer function of N path $G_m - C$ canceller when Gm = 0 mS can be obtained from [12]

$$|\frac{I_{canceller}}{V_{in}}| \approx \frac{8}{\pi^2}\frac{R_l + R_{on}\omega_s C_c R_0}{R_s + R_l + 2R_{on}} \tag{3.2}$$

From (3.2), it is observed that variable attenuation can be obtained by changing R_s and R_l. The effect of R_s on the magnitude of the transfer function is shown in Fig. 3.4. The transconductance Gm is used to shift the center frequency of the filter, as shown in Fig. 3.4. The required frequency shift range $\Delta\omega$ is $\frac{Gm}{C_B}$ as given in [40]. 2-port N-path filter has an interesting property of embedded phase shifting. The phase response of the filter can be tuned by applying LO phase shift to the clock signals, which drive the output switches. The separation between two clock signals Δt determines the phase shift in the cancellation signal $I_{canceller}$ shown in Fig. 3.4. The amplitude and phase of N-path $G_m - C$ filter can be tuned independently.

The differential N-path $G_m - C$ filters are used to achieve high IIP2. This receiver has a noise-canceling common-gate common-source low noise transconductance amplifier (LNTA). The SI cancellation is tested by antenna pairs at the receiver and transmitter end. A 27 MHz bandwidth 64 QAM signal is transmitted using an off-chip power amplifier at 1.4 GHz. The modulated SI appears at the receiver input with 35 dB antenna isolation. A 20 dB cancellation is measured across the entire 27 MHz SI bandwidth. In FD mode SI cancellation increases the effective IIP3 and IIP2 by 22 dB and 58 dB, respectively. The gain compression increases to -8 dBm.

3.2.2 Passive vector modulator [13]

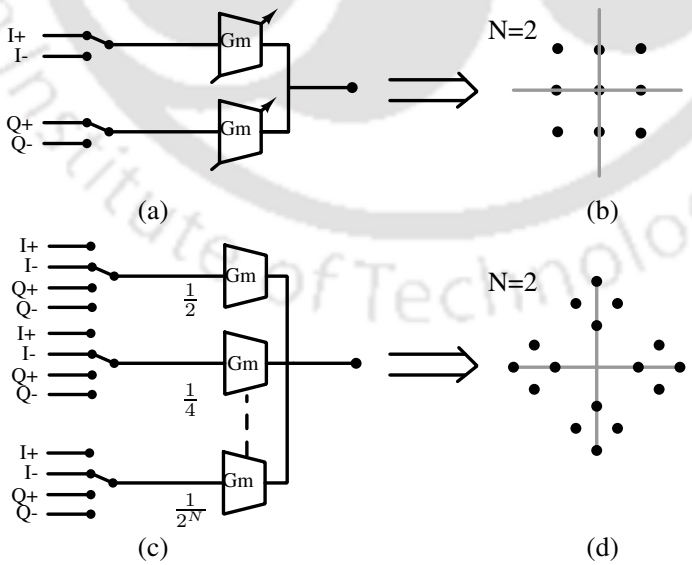


Figure 3.5: (a) Conventional vector modulator. (b) Constellation diagram of conventional vector modulator. (c) Vector modulator [41]. (d) Constellation diagram of vector modulator [41].

A Vector modulator generates an output signal with adjustable magnitude and phase from the

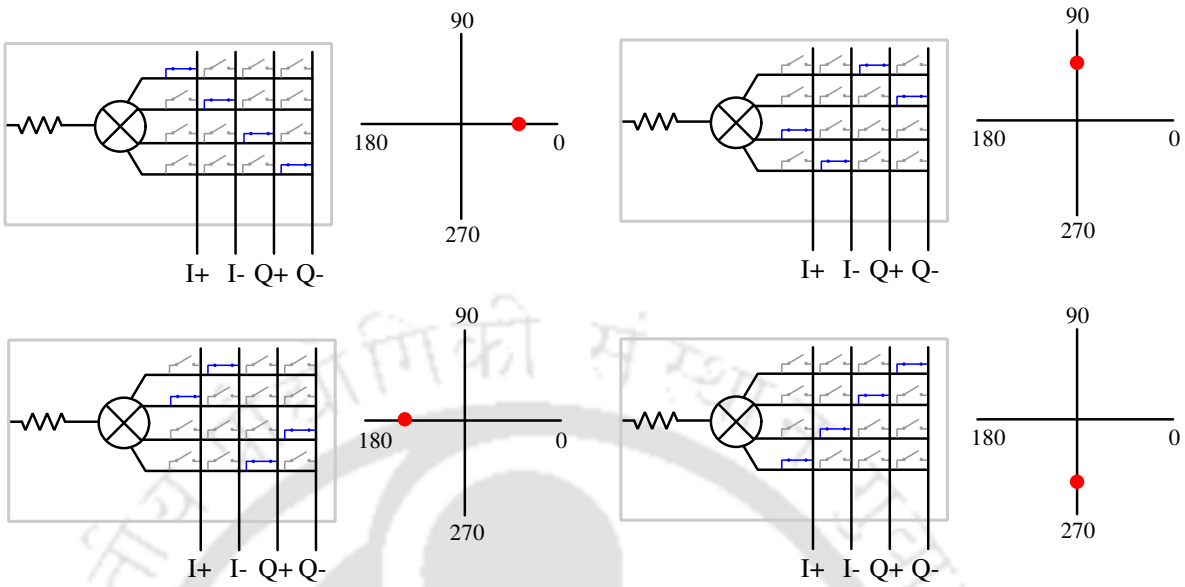


Figure 3.6: Constellation diagram of passive vector modulator [13].

addition of two 90 degrees out of phase I and Q signals. The conventional vector modulator is shown in Fig. 3.5(a), where digitally controllable transconductors are used to I and Q vectors. Each point in the constellation diagram is the weighted sum of I and Q vectors. The number of constellation points depends on the transconductance range. The fine resolution of the constellation diagram can be achieved by allowing a small step size of Gm value. Each quadrant can be selected by changing the polarities of I and Q using static switches. N represents the number of discrete levels of Gm. For example, if N=2, the number of possible constellation points are nine as shown in Fig. 3.5(b). The main drawback of this modulator is that the output impedance of transconductance changes with Gm value. The vector modulator [41] has fixed Gm stages as shown in Fig. 3.5(c). Each transconductance stage is assigned to a binary-weighted value of $\frac{1}{2^N}$, where N is the number of stages. For example if N=2 then Gm values will be $\frac{1}{2}$ and $\frac{1}{4}$.Each transconductance stage is connected to I+, I-, Q+ and Q- through switches. The number of possible constellation points is 16 as shown in Fig. 3.5(d).

The implementation of the passive vector modulator downmixer [13] is similar to the transconductance vector modulator [41] with the only difference; it has only switches and no gm stages. The number of constellation points depend on the number of slices used in vector modulator. For n slices there are $n+1 \times n+1$ points in the constellation diagram. Fig. 3.6 shows the implementation of a passive vector modulator. The vector modulator should cover all phases in a circle and provides a sufficient range

of attenuation for SI cancellation. The minimum SI cancellation depends on the quantization error of the constellation. The minimum SI cancellation is given as

$$\text{SIC(dB)} = 20\log_{10}(n+1) - 3 \text{ dB} \tag{3.3}$$

31 slice are used to achieve a minimum cancellation of 27 dB. Whenever the vector modulator is disabled, it acts as a conventional mixer first receiver. The maximum amplitude is obtained when all slices are set to the same phase, i.e 0°, 90°, 180° and 270°. The minimum amplitude is obtained when half of the slices are set to 180 out of phase to the other half.

The performance SI cancellation is tested by using over 100 different amplitude/phase signals. The cancellation is measured for each vector modulator setting, and an algorithm based on power minimization is used to find the amount of cancellation. The worst-case cancellation achieved is 27 dB. The peak SINDR is 70.5 dB in 16.25 MHz bandwidth. The maximum SI power that can be applied to this receiver is -16.4 dBm. The effective IIP3 and IIP2 are 21.5 dBm and 60 dBm, respectively.

3.2.3 Adaptive double cancellation [14]

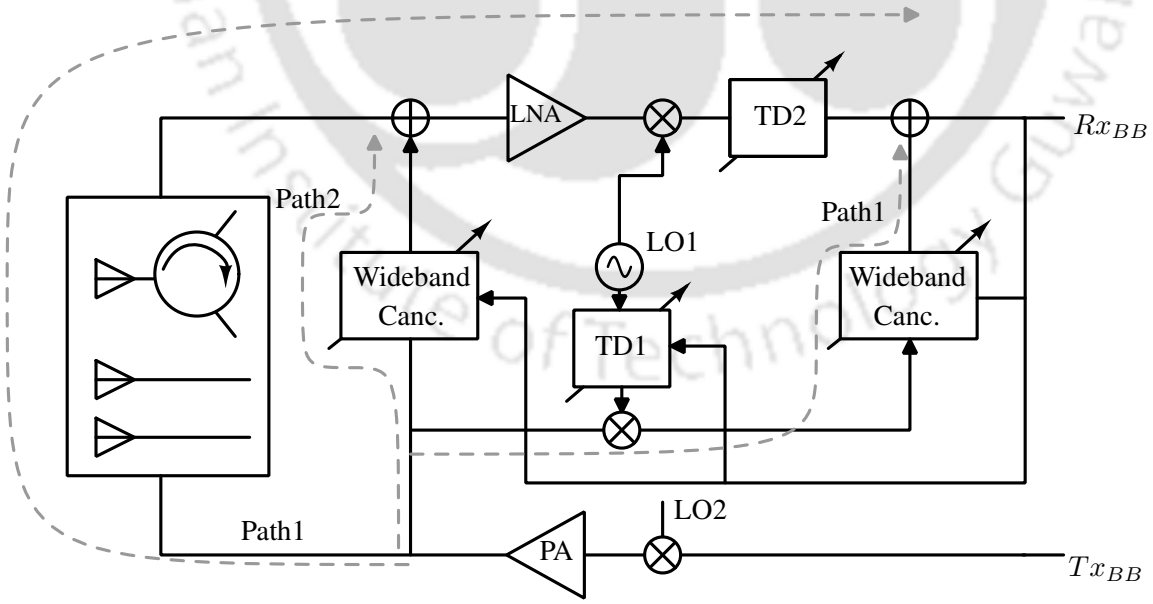


Figure 3.7: Block diagram of the FD front-end for wide-band SI cancellation [14].

This FD system [14] has two wideband cancellation paths, one at RF, while the second one is in baseband, as shown in Fig. 3.7. The adaptive filters are used to create an inverse time-domain response

of the leakage path to track a time-varying response. The analog RF canceller is implemented as an analog FIR filter, where each tap has a true-time-delay (TTD) circuit, a buffer, and a 7-bit variable-gain amplifier (MSB determines the polarity, while the other 6 bits control the canceller gain). The TTD block is designed as an RC-CR all-pass filter. Each of the RF TTD blocks provides a fixed simulated time delay. The variable-gain amplifier is designed with a set of low-power, low-noise inverter-based Gm stages. The current output of each tap is summed and fed to the receiver input. There is a tradeoff between bandwidth and NF degradation. More filter taps increase the cancellation bandwidth, but degrade the receiver NF and raise the power consumption. The baseband canceller design uses a 14-tap adaptive filter. Each of the baseband TTD blocks is similar to [42] and has a simulated 10 ns time delay. The mixers used in the receiver signal chain and baseband canceller paths (path 3) utilize the same LO signal (LO1), but have a delay mismatch between them. Thus, a variable delay (TD1) in the LO output that supplies the path-3 mixer, compensates for the path 1- to-3 delay mismatch. Combining the baseband canceller and TD1 allows the suppression of both the transmitter SI and receiver LO sidebands.

3.3 Proposed full-duplex receiver

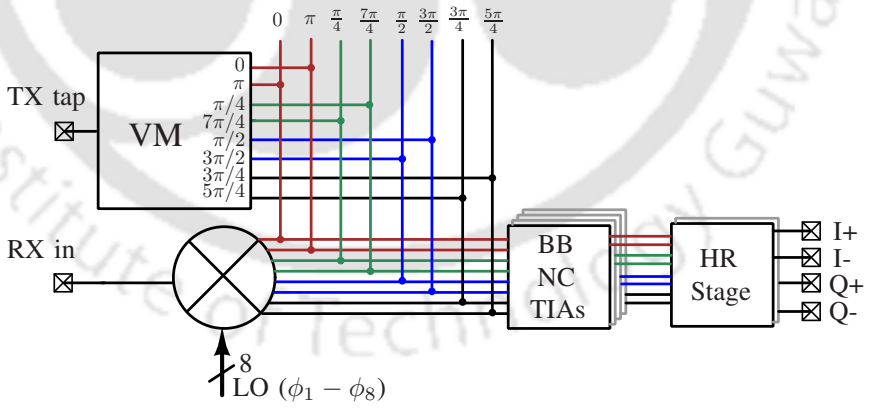


Figure 3.8: Architecture of the proposed full-duplex receiver.

The proposed FD receiver is shown in Fig. 3.8. The receiver path consists of an eight-path passive mixer followed by a set of trans-impedance amplifiers (TIA). A harmonic recombination (HR) circuit is used at the output to reject the signals from the third and fifth harmonic frequencies [43, 44]. N-path mixer-first receivers offer clock-tunable narrowband RF filtering at the receiver input due to their frequency translational property. The proposed SI canceller is based on a cross-domain vector

modulator (VM) with an RF-input and 'N' number of IF-outputs. The 'N' outputs of the VM and the 'N' outputs of the mixer in the receiver path are combined as shown in Fig. 3.8 to cancel the self-interference.

3.3.1 Vector modulator

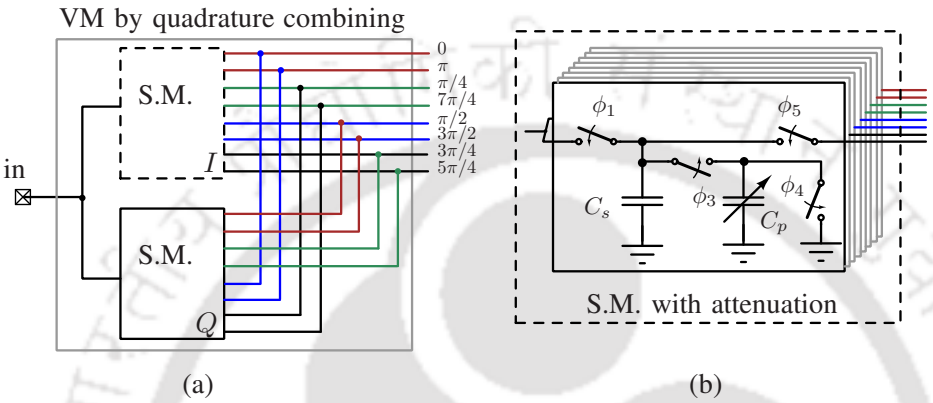


Figure 3.9: Proposed (a) Cartesian vector modulator and (b) the N-path sampling mixer with variable attenuation.

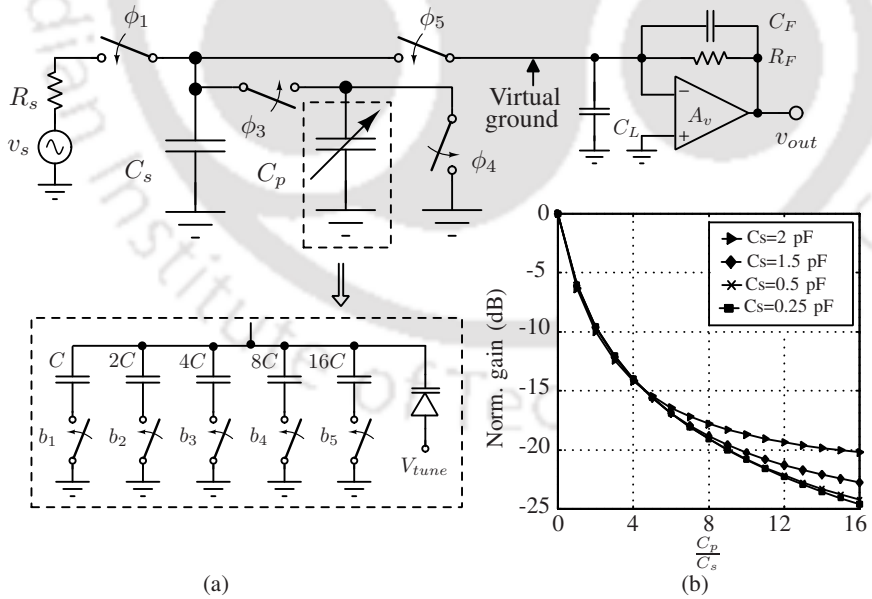


Figure 3.10: (a) One path of the N-path sampling mixer with variable attenuation, and the realization of the variable capacitor. (b) Attenuation of the signal with the ratio $\frac{C_p}{C_s}$.

The key building block in the proposed VM is an N-path sampling mixer (SM) with variable attenuation. The outputs of two N-path sampling mixers are combined in quadrature to form a VM

as shown in Fig. 3.9(a). Fig. 3.9(b) shows the N-path sampling mixer with variable attenuation. In Fig. 3.9(b), C_s is the sampling capacitor, C_p is the variable attenuation capacitor, and ϕ_i, $i = 1, 2, \ldots, 8$ represent the eight non-overlapping clocks each having 12.5% duty cycle.

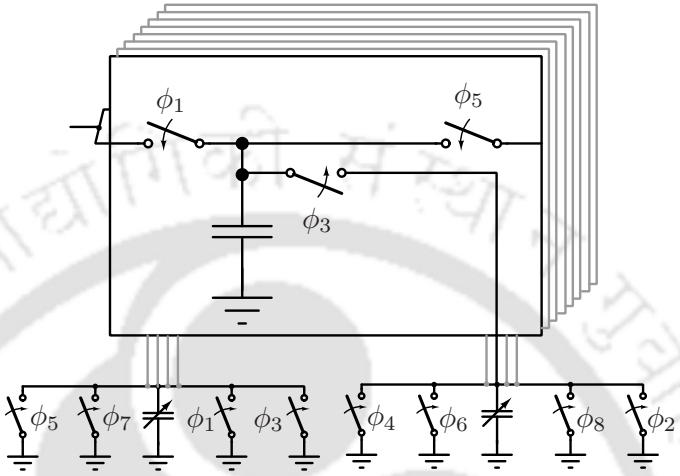


Figure 3.11: Sharing one capacitor bank among four-paths. In an eight-path canceller, two capacitor banks are sufficient.

The operation of the N-path sampling mixer with variable attenuation can be explained with the help of the single-path shown in Fig. 3.10(a). During the clock phase ϕ_1, the input voltage v_s is sampled onto a capacitor C_s. In the clock phase ϕ_3, an uncharged capacitor C_p is connected in parallel with the already charged ($Q = C_s v_s$) capacitor C_s. This parallel connection results in charge sharing between C_s and C_p, and the voltage across the parallel combination drops to $\frac{C_s v_s}{C_s+C_p}$. During the clock phase ϕ_4, the parallel capacitor C_p is disconnected from the sampling capacitor C_s. Moreover, C_p is discharged in ϕ_4. In the clock phase ϕ_5, the sampling capacitor C_s with a residual charge of $\frac{C_s^2 v_s}{C_s+C_p}$ is connected to the virtual ground at the input of the baseband (BB) trans-impedance amplifier (TIA). One can notice that the input voltage v_s is attenuated by $\frac{C_s}{C_s+C_p}$ before it is being fed to the BB TIA. If C_p can be varied continuously, continuous range of attenuation levels can be achieved. Fig. 3.10(a) also shows a possible realization of the continuously tunable parallel capacitor C_p using a combination of digitally tunable capacitors and a varactor. Fig. 3.10(b) shows the simulated attenuation with varying C_p/C_s ratio.

The eight-path sampling mixer with variable attenuation shown in Fig. 3.9(b) requires eight parallel capacitors (which means eight capacitor banks) C_p. In a given path of the mixer (Fig. 3.10(a)), the parallel capacitor C_p is used only during one clock phase (ϕ_3). In the immediately next clock phase

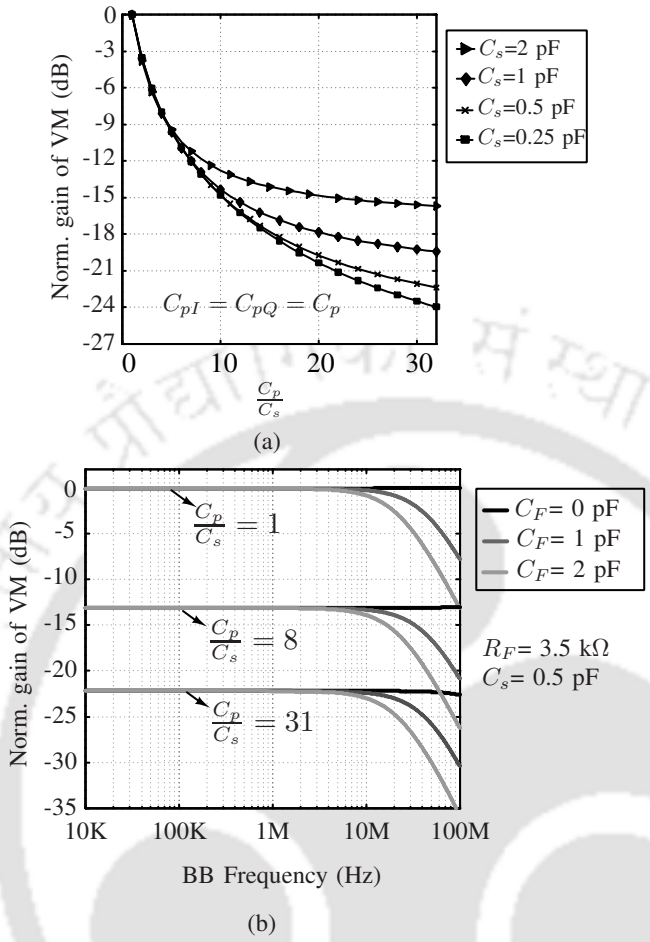


Figure 3.12: (a) VM output magnitude variation with $\frac{C_p}{C_s}$ for different C_s. (b) Effect of TIA bandwidth on the magnitude response of the VM.

(ϕ_4), C_p is fully discharged and ready to be reused. In an eight-path sampling mixer, a single capacitor C_p can be shared among four paths (among all even paths or among all odd paths). Fig. 3.11 shows the modified version of the mixer in Fig. 3.9(b) which requires only two shared capacitor banks.

The two sampling mixers in the VM act as I-canceller and Q-canceller mixers. Further, the magnitudes of the I-canceller and Q-canceller outputs can be varied continuously and independently. The proposed VM downmixer is simulated with ideal switches and ideal TIAs. Fig. 3.12(a) shows the normalized gain at the output of the TIAs at a given frequency for different $\frac{C_p}{C_s}$ ratios. The gain plot in Fig. 3.12(a) can also be seen as the magnitude variation of a canceller signal at a given frequency at 45° phase angle. Fig. 3.12(b) shows the effect of the TIA feedback capacitor C_F on the magnitude response. Fig. 3.13(a) shows the normalized output phase (referenced with 45°) variation with respect to the ratio of the attenuation capacitors in I-and-Q cancellers ($\frac{C_{pQ}}{C_{pI}}$). Fig. 3.13(b) shows

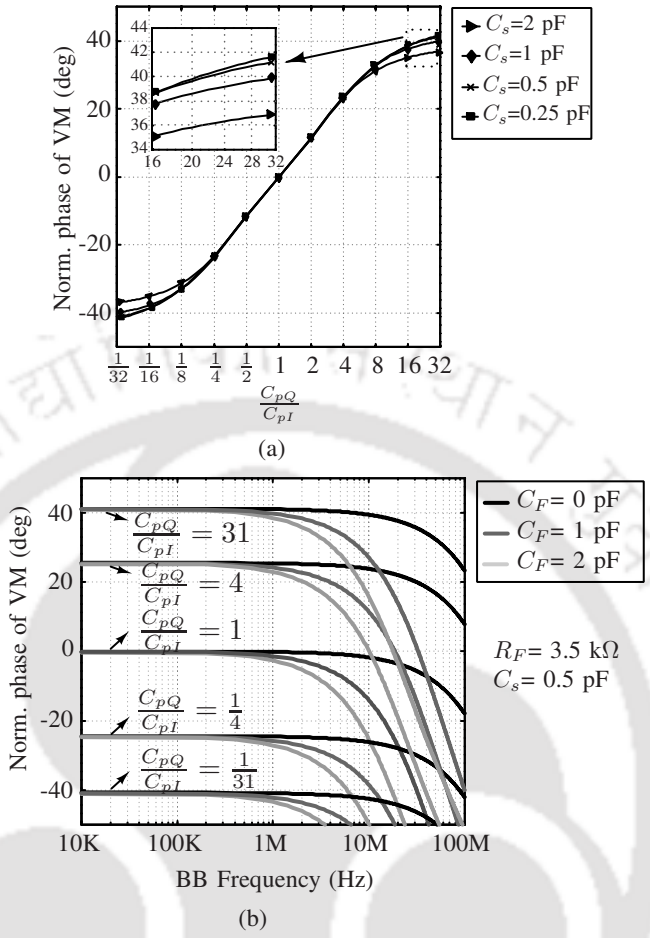


Figure 3.13: (a) VM output phase variation with $\frac{C_{pQ}}{C_{pI}}$ for different C_s. (b) Effect of TIA bandwidth on the phase response of the VM.

the effect of the TIA feedback capacitor C_F on the phase response of the VM. From Fig. 3.12(b) and Fig. 3.13(b), the operational bandwidth of the proposed canceller path is limited by the TIA bandwidth $f_{3dB,TIA} = \frac{1}{2\pi R_F C_F}$ [1]. Fig. 3.14(a) shows the simulated constellation points of the proposed VM with an ideal 4-bit capacitor bank. The dead-zones near the I-and-Q axes are due to the finite ON-capacitance C_p in each canceller. Fig. 3.14(b) shows the constellation region bounded by the four outer discrete constellation points that is covered with the help of varactors in I-and-Q cancellers.

3.3.1.1 Resolution

Let the C_p/C_s ratio in the I-canceller be x and the C_p/C_s ratio in the Q-canceller be y. Then the attenuation of the I-canceller is $\alpha(x) = \frac{1}{1+x}$ and the attenuation of the Q-canceller is $\beta(y) = \frac{1}{1+y}$. The

[1]Since the I-and-Q cancellers are sampling mixers, the 3-dB bandwidth of VM without TIA is $\approx \frac{f_s}{2}$, where f_s is the clock frequency [39].

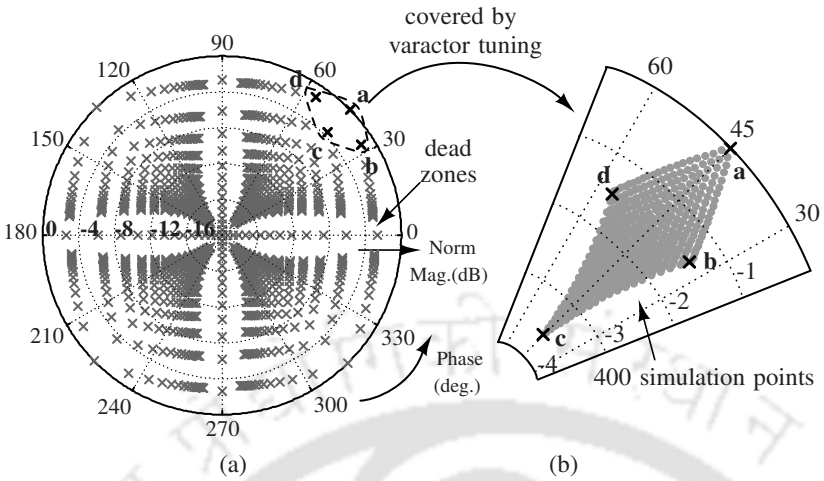


Figure 3.14: (a) Discrete constellation points due to the 4-bit capacitor banks in the VM and (b) the constellation region bounded by the four outer discrete constellation points that is covered by the varactors of the VM.

final output of the proposed VM can be expressed as

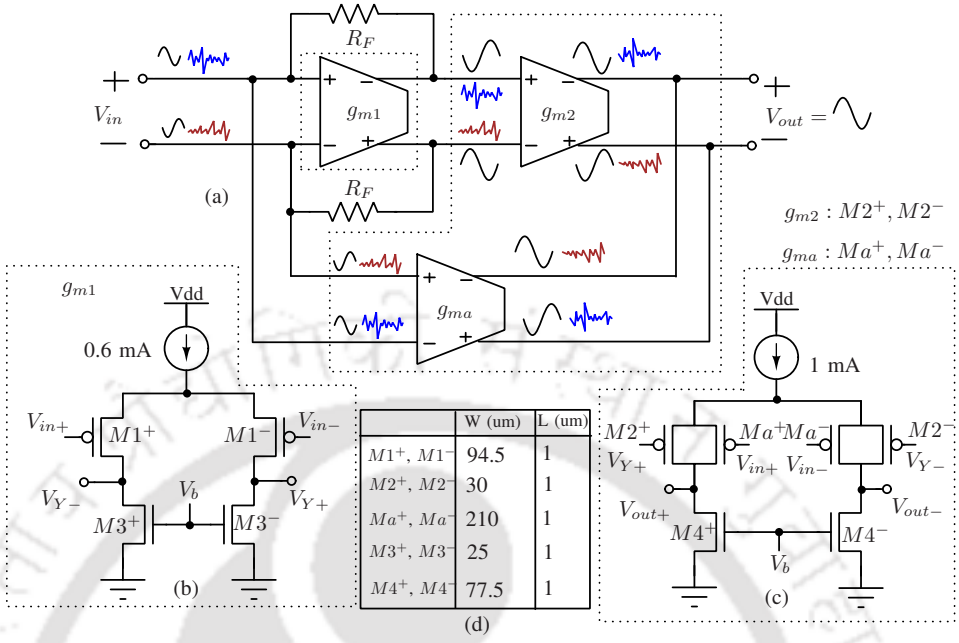
$$\begin{aligned} H_{VM} &= \alpha(x) + j\beta(y) \\ &= \sqrt{\alpha^2(x) + \beta^2(y)} \;\; \angle tan^{-1}\left[\frac{\beta(y)}{\alpha(x)}\right]. \end{aligned} \tag{3.4}$$

One can cover the complete region in the constellation diagram only if $\frac{C_p}{C_s}$ can be varied from 0 to ∞. If $(\frac{C_p}{C_s})_{max} = k$, then the output of the VM with the maximum attenuation setting in the Q-canceller is

$$H_{VM} = \sqrt{\alpha^2(x) + (\frac{1}{1+k})^2} \;\; \angle \tan^{-1}\left[\frac{1+x}{1+k}\right] \tag{3.5}$$

As x varies from 0 to k, (3.5) gives the set of constellation points that are close to the I-axis. The empty region between these points and the I-axis becomes the dead-zone of the VM. Similar dead-zones exist on both sides of Q-axis as shown in Fig. 3.14. One has to choose large $(C_p/C_s)_{max}$ ratio to reduce the dead-zone phase. One way to mitigate the problem of dead-zones is to rotate the constellation diagram by $\pm 45°$ when an SI falls in the dead-zone. This can be achieved by reconfiguring[2] the mixer and VM connections (shown in Fig. 3.8) such that the $\pm 45°$ output of the mixer is connected to the $0°$ output of the VM.

[2]This is not implemented in the current work.



	W (um)	L (um)
$M1^+$, $M1^-$	94.5	1
$M2^+$, $M2^-$	30	1
Ma^+, Ma^-	210	1
$M3^+$, $M3^-$	25	1
$M4^+$, $M4^-$	77.5	1

Figure 3.15: (a) Block-level view of the baseband noise canceling TIA. Transistor-level schematics of the (b) first and (c) second stages of the TIA. (d) Dimensions of the transistors used in this work.

3.3.2 Noise canceling TIA

Since TIA is the first gain block in a passive mixer-first receiver, the noise contribution of the TIA to the overall receiver noise is significant. To reduce the noise contribution of the TIA, noise cancellation [45–51] is exploited in the baseband TIA. Fig. 3.15(a) shows the block diagram of the fully-differential noise canceling TIA that is used in this work. In the shunt feedback TIA realized using the g_{m1} stage and the feedback resistors R_F, the instantaneous noise voltages at the input and output are in-phase whereas the signal voltages at the input and output are out-of-phase. If we add a second stage g_{m2} and an auxiliary stage g_{ma} as shown in Fig. 3.15(a), the noise voltage due to g_{m1} can be canceled at the differential output V_{out}. The TIA is dc coupled to the mixer and the VM block. A high dc voltage at the input of the TIA will reduce the V_{GS} of switches (of mixer and VM) when they are ON and this causes an increase in the ON-resistance of the switches. The two possible solutions to this problem are either level shifting the clock signals or ensuring a low dc voltage at the input of the TIA. All stages in the TIA are implemented using pMOS differential pairs to ensure low dc voltage at the output of the VM. Fig. 3.15(b) and Fig. 3.15(c) show the transistor-level implementations of g_{m1}, g_{m2}, and g_{ma}. Fig. 3.15(d) shows the dimensions of the transistors used in this work. For noise cancellation, we need $g_{ma} > g_{m2}$. The detailed noise analysis is presented in Section 3.4.3.

3.3.3 Other blocks

The switches in the passive mixer are implemented using nMOS transistors. A single-stage amplifier based weighted summer is used as the HR stage. The VM shown in Fig. 3.9 can generate a canceller signal with a phase angle $0 < \theta < \frac{\pi}{2}$. To generate the signals with phase angle between $\frac{\pi}{2}$ and 2π, we have added phase reversal switches at the outputs of I and Q cancellers in the VM. A frequency divider based on D flip-flops is used to generate the eight non-overlapping clock signals from an externally-fed clock.

3.4 Receiver analysis

3.4.1 Input impedance

Impedance translational properties of passive mixer-first receivers are studied in detail in [52], and proposed an equivalent LTI model as shown in Fig. 3.16(a). In Fig. 3.16(a), R_s is the source resistance, R_{sw} is the ON-resistance of the switch, R_{sh} accounts for the power lost due to up-conversion of the input signal, R_B represents the resistance looking into the TIA input, C_L represents the shunt capacitance at the TIA input, and γ represents a constant that depends on the number of paths. In Fig. 3.16(a), the impedance Z_{BB} represents the baseband impedance and should be evaluated at the intermediate frequency $(\omega_{RF} - \omega_{LO})$. From the model in Fig. 3.16(a), the input impedance Z_{in} of the receiver around the fundamental frequency is given by

$$\begin{aligned} Z_{in} &= R_{sw} + R_{sh} || \gamma Z_{BB}, \\ &= R_{sw} + \frac{1}{\frac{1}{R_{sh}} + \frac{1}{\gamma R_B} + j(\omega_{RF} - \omega_{LO})\frac{C_L}{\gamma}}, \end{aligned} \tag{3.6}$$

where

$$\gamma = \frac{sinc(\frac{\pi}{N})^2}{N}, \tag{3.7}$$

and

$$R_{sh} = (R_s + R_{sw})\frac{N\gamma}{1 - N\gamma}. \tag{3.8}$$

For the proposed noise canceling TIA shown in Fig. 3.16(b), the impedance $R_B \approx 1/g_{m1}$. Fig. 3.17 shows a comparison of simulated and analytical (3.6) input impedance. From Fig. 3.17(a), the g_{m1} required for 50 Ω input match is approximately 3mʊ.

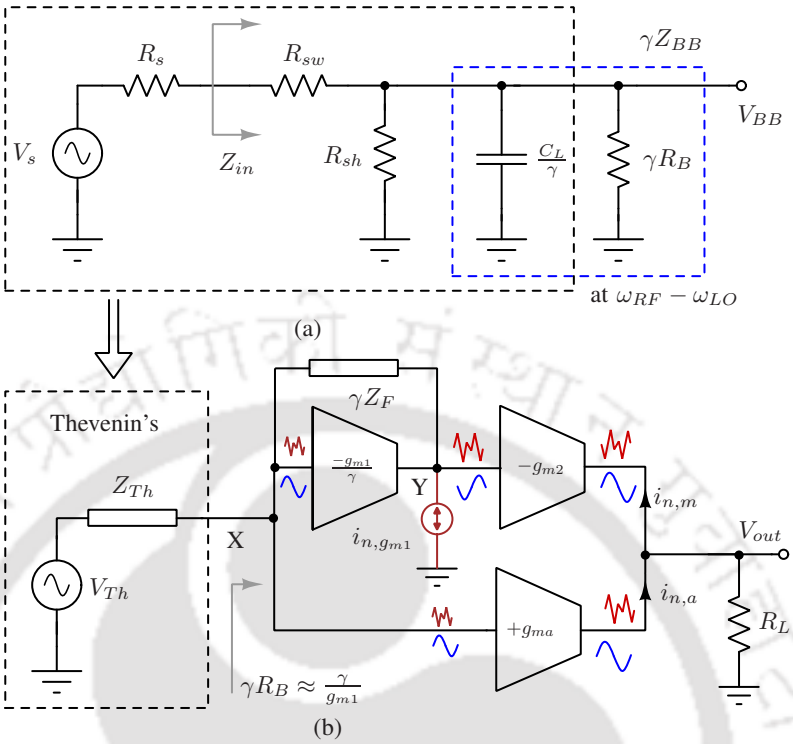


Figure 3.16: (a) Equivalent LTI model of N-path mixer-first receivers. (b) Input impedance of the TIA per path.

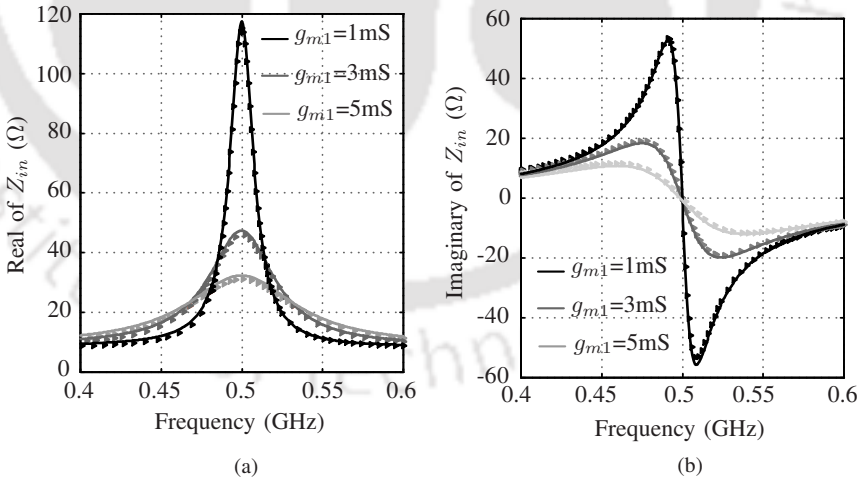


Figure 3.17: Comparison of simulated and analytical (3.6) (a) real and (b) imaginary parts of the input impedance when $f_{LO} = 500$MHz. Marker indicates the analytical results and solid line indicates the simulated results.

3.4.2 Gain

To compute the conversion gain of the receiver, the LTI model shown in Fig. 3.16(a) is modified to the one shown in Fig. 3.16(b). In Fig. 3.16(b), the baseband resistance γR_B is replaced by an equivalent single-ended noise canceling TIA with appropriate scaling factors and the network in-front of the TIA is replaced by an equivalent Thevenin network. The Thevenin voltage (V_{Th}) and the open-circuit impedance (Z_{Th}) are

$$V_{Th} = \frac{R_{sh}||\frac{\gamma}{j\omega_{IF}C_L}}{R_a + R_{sh}||\frac{\gamma}{j\omega_{IF}C_L}} V_s, \tag{3.9}$$

$$Z_{Th} = R_a||R_{sh}||\frac{\gamma}{j\omega_{IF}C_L},\ where\ R_a = R_s + R_{sw}. \tag{3.10}$$

The voltages at nodes X, Y and output are

$$V_X = \frac{1}{1+\frac{g_{m1}}{\gamma}Z_{Th}}\ V_{Th}, \tag{3.11}$$

$$V_Y = \frac{1-g_{m1}Z_F}{1+\frac{g_{m1}}{\gamma}Z_{Th}}\ V_{Th}, \tag{3.12}$$

$$\begin{aligned} V_{out} &= (-g_{m2}V_Y + g_{ma}V_X)R_L \\ &= \left[\frac{-g_{m2}(1-g_{m1}Z_F)+g_{ma}}{1+\frac{g_{m1}}{\gamma}Z_{Th}}\right]V_{Th}R_L \end{aligned} \tag{3.13}$$

The voltage gain of the receiver is

$$G = \frac{V_{out}}{V_s} = \left[\frac{-g_{m2}(1-g_{m1}Z_F)+g_{ma}}{1+\frac{g_{m1}}{\gamma}Z_{Th}}\right]\frac{Z_{Th}}{R_a}R_L \tag{3.14}$$

Fig. 3.18(a) shows a comparison of the simulated and analytical (3.14) voltage gains of the receiver for different g_{ma}/g_{m2} ratios at $f_{RF} = 500$ MHz. In this simulation the following parameters are used: $R_{sw} = 8\ \Omega$, $R_L = 1\ \text{k}\Omega$, $C_L = 20$ pF, $g_{m1} = 2.8$ m℧, $g_{m2} = 1$ m℧, and $Z_F = 3.5\ \text{k}\Omega\ ||\ \{0\text{ pF}, 4\text{ pF}\}$.

3.4.3 Noise

3.4.3.1 Noise canceling condition

In the proposed NC TIA, only the noise of g_{m1} can be canceled at the output. In Fig. 3.16(b), $\overline{i_{n,g_{m1}}}$ represents the noise current due to g_{m1}. The instantaneous noise voltages at nodes X and Y

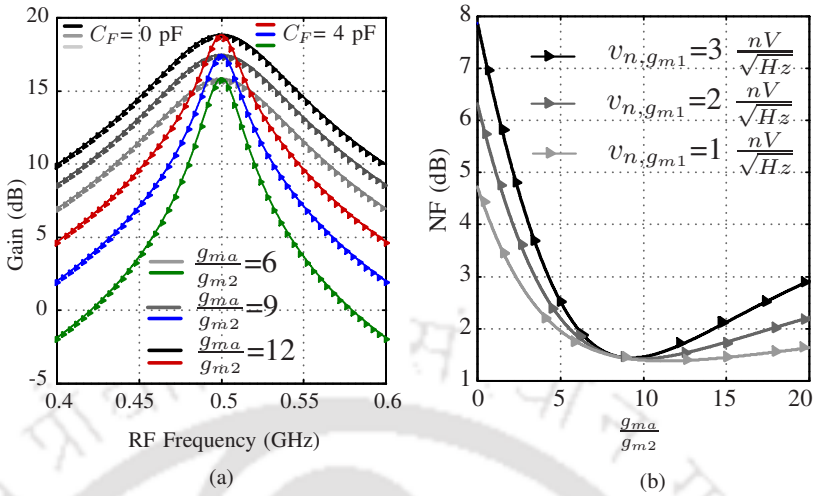


Figure 3.18: Comparison of simulated and analytical (a) voltage gain and (b) NF of the receiver using ideal transconductors. Marker indicates the analytical results and solid line indicates the simulated results.

due to $\overline{i_{n,g_{m1}}}$ are

$$v_{n,X} = \frac{\overline{i_{n,g_{m1}}}}{\sqrt{\gamma}} \frac{Z_{Th}}{1+\frac{g_{m1}}{\gamma}Z_{Th}} \tag{3.15}$$

$$v_{n,Y} = \frac{\overline{i_{n,g_{m1}}}}{\sqrt{\gamma}} \frac{Z_{Th}+\gamma Z_F}{1+\frac{g_{m1}}{\gamma}Z_{Th}} \tag{3.16}$$

For noise cancellation at the output, the noise currents at the outputs of g_{m2} and g_{ma} should be equal in magnitude.

$$g_{ma}\frac{\overline{i_{n,g_{m1}}}}{\sqrt{\gamma}} \frac{Z_{Th}}{1+\frac{g_{m1}}{\gamma}Z_{Th}} = g_{m2}\frac{\overline{i_{n,g_{m1}}}}{\sqrt{\gamma}} \frac{Z_{Th}+\gamma Z_F}{1+\frac{g_{m1}}{\gamma}Z_{Th}}$$

$$\frac{g_{ma}}{g_{m2}} = 1+\frac{\gamma Z_F}{Z_{Th}} \tag{3.17}$$

If Z_F is a parallel combination of a resistor R_F and a capacitor C_F, then $Z_F \approx R_F$ and $Z_{Th} \approx R_a||R_{sh}$ in the passband, (3.17) can be written as

$$\frac{g_{ma}}{g_{m2}} = 1+\frac{\gamma R_F}{R_a||R_{sh}} \tag{3.18}$$

From (3.14) and (3.18), the voltage gain under the noise-canceling condition is

$$G_{NC} = g_{m2}\frac{\gamma R_F R_L}{R_a} \tag{3.19}$$

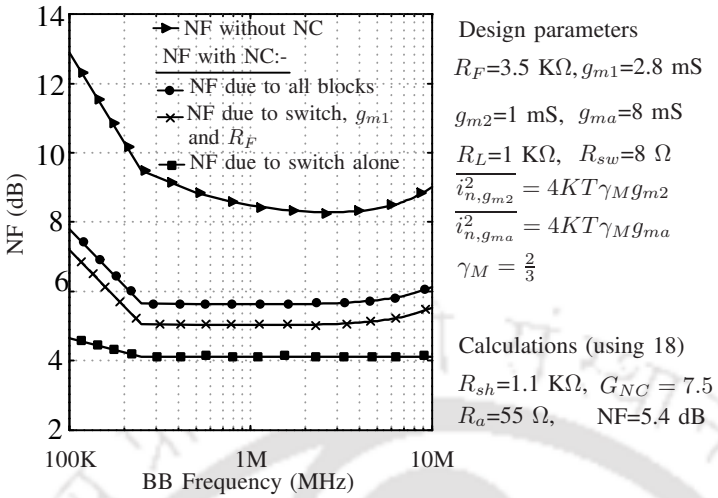


Figure 3.19: NF of the receiver with and without noise cancellation.

The noise canceling condition (3.18) is verified through the simulation of a receiver with an ideal g_{m2} stage having different input referred noise voltages. In this simulation, $R_F = 3.5$ kΩ, $R_{sw} = 8$ Ω, R_L =1 kΩ, $C_L = 20$ pF, $g_{m1} = 2.8$ mʊ and $g_{m2} = 1$ mʊ are used. Fig. 3.18(b) shows the variation of NF with $\frac{g_{ma}}{g_{m2}}$.

3.4.3.2 Noise Factor

Let $\overline{v^2_{n,s}} = 4kTR_s$, $\overline{v^2_{n,sw}} = 4kTR_{sw}$, $\overline{v^2_{n,sh}} = 4kTR_{sh}$ and $\overline{v^2_{n,f}} = 4kT\gamma R_F$ represent the mean square thermal noise voltage densities of the resistors R_s, R_{sw}, R_{sh} and R_F respectively. Let $\overline{i^2_{n,g_{m2}}}$, and $\overline{i^2_{n,g_{ma}}}$ represent the mean square thermal noise current densities at the outputs of g_{m2} and g_{ma} respectively. The noise due to g_{m1} is not considered as it is cancelled at the output.

The total noise voltage across R_L is

$$\overline{v^2_{n,out}} = G^2_{NC}\left(\overline{v^2_{n,s}} + \overline{v^2_{n,sw}} + \left[\frac{R_a}{R_{sh}}\right]^2 \overline{v^2_{n,sh}}\right) + g^2_{m2}R^2_L\overline{v^2_{n,f}} + \overline{i^2_{n,gm_2}}R^2_L + \overline{i^2_{n,gm_a}}R^2_L, \tag{3.20}$$

Using (3.19), the noise factor (NF) can be computed as

$$NF = 1 + \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left[\frac{R_a}{R_{sh}}\right]^2 + \frac{R^2_a}{\gamma R_F R_s} + \frac{1}{G^2_{NC}4kTR_s}\left(\overline{i^2_{n,gm_2}} + \overline{i^2_{n,gm_a}}\right)R^2_L \tag{3.21}$$

Fig. 3.19 shows the NF of the receiver with and without noise cancellation using ideal switches and ideal TIAs. The NF can be calculated from the design parameters shown in Fig. 3.19 and (3.21). The calculated NF is 5.4 dB and the simulated NF of the receiver is 5.7 dB.

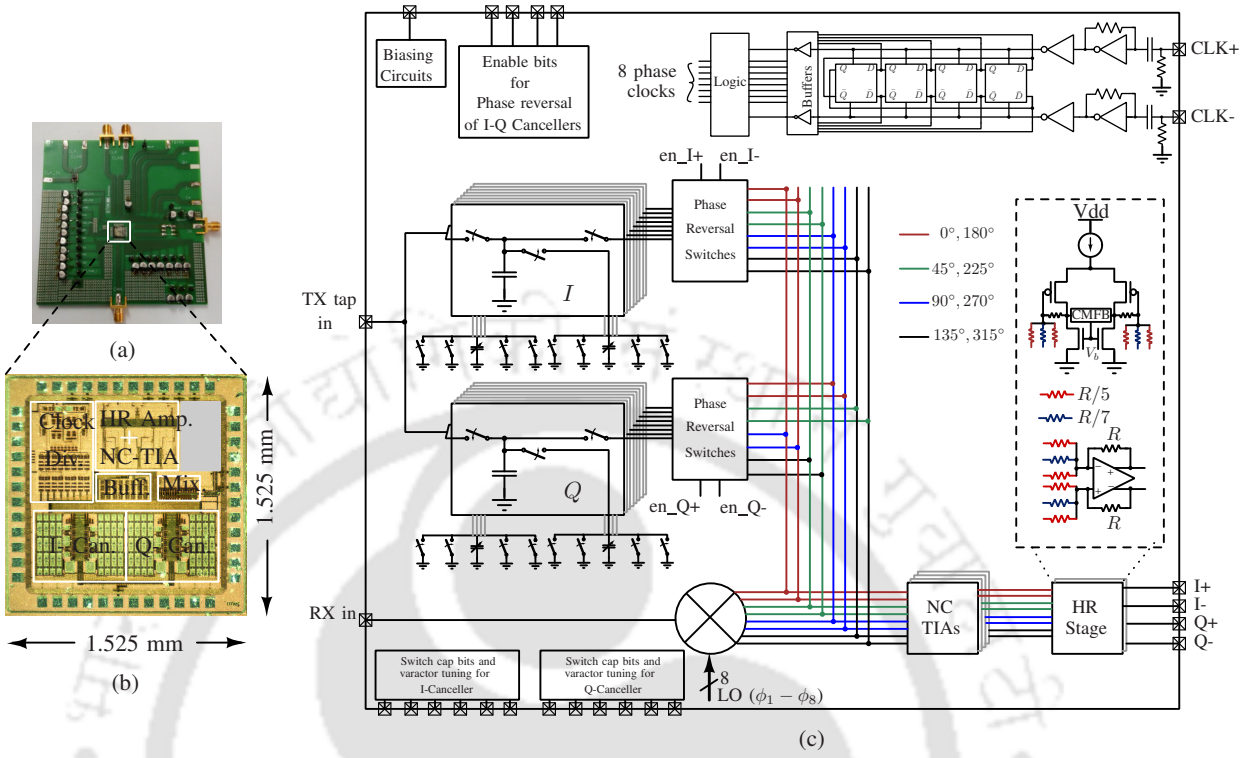


Figure 3.20: (a) Testing board, (b) chip photograph, and (c) block level architecture of the implemented chip.

3.4.4 Linearity

In general, passive current driven mixers are highly linear in nature. The typical IIP3 value is more than 20 dBm for a switch resistance of 20 Ω [13]. In most of the mixer-first receivers, TIA limits the in-band linearity of the receiver. In particular, the IIP3 of the last amplifying stage dominates the IIP3 of the complete receiver. In the current implementation, the harmonic recombination block limits the linearity of the receiver as it experiences a large-signal at its input. One should note that the noise cancellation technique also cancels the distortion due to the g_{m1} stage [45]. One possible way to increase the linearity of the baseband amplifiers is to operate them on a higher supply voltage as in [14].

3.5 Implementation details

A prototype FD receiver is implemented in a CMOS 130 nm technology. The chip is enclosed in a 48-pin QFN package and mounted on a board for testing. The photographs of the testing board and the chip are shown in Fig. 3.20(a) and Fig. 3.20(b) respectively. The complete block level architecture

of the chip is shown in Fig. 3.20(c). The mixer switches are optimized for better linearity and moderate power consumption [52]. The ON resistance of the switches is also 8 Ω. The proposed NC differential TIAs are used in the receiver. The transconductance of the main amplifiers (g_{m1}) is tuned to achieve a good 50 Ω input match. The ratio of the transconductance of the forward to the auxiliary amplifier is set based on the NC condition. One μm channel length devices are used in all baseband circuits to reduce the Flicker noise at low offset frequencies.

The I-and-Q cancellers of the VM downmixer, are eight-path sampling mixers with a sampling capacitance of 0.5 pF. The variable capacitor in each sampling mixer is implemented by a combination of 5-bit binary-weighted MIM capacitor-bank and a MOS varactor. A single bit in the capacitor-bank corresponds to 0.5 pF and the varactor has a tuning range of ≈ 1.1 pF. The range of the attenuation capacitance values (C_{max} to C_{min}) mainly depends on the size of the switches. The size of the switches in the capacitor bank is chosen based on the trade-off between the quality factor (Q) and the capacitance range. The size of VM switches affect the magnitude and phase responses of the VM (Fig. 3.12 and Fig. 3.13). As the VM switch size increases, the OFF capacitance of the switch increases which leads to a reduction in the dynamic range (ratio of maximum to minimum attenuation) of the VM. In a given CMOS technology, the product of ON-resistance (R_{on}) and OFF-capacitance (C_{off}) of a switch is a constant [2]. A small switch size will have large R_{on}, and hence increases the time constant of the sampler. Therefore, there is a trade-off between the maximum frequency of operation of the VM and the dynamic range of the VM. According to Peregrines switch road-map [2], lower CMOS technology nodes will have switches with lower $R_{on}C_{off}$. In the current implementation a switch size of $\frac{64\ \mu m}{0.12\ \mu m}$ ($R_{on} = 8\ \Omega$ and $C_{off} \approx 65$ fF) is found to be an optimal choice.

The 12.5% duty cycle non-overlapping clock signals are generated by divide-by-four and combinational logic circuits. The mixer and canceler switches are driven by the same clock signals.

3.6 Measurement results and discussion

3.6.1 When the SI canceller is OFF

The receiver is tunable from 0.1 to 0.95 GHz. Fig. 3.21(a) shows variation of the gain and NF with the local oscillator (LO) frequency. Over the tuning range of 0.1-0.95 GHz, the receiver has a conversion gain > 37 dB and NF < 8 dB. The receiver has a bandwidth of ≈ 8 MHz. Fig. 3.21(b) shows the IB input referred third-order intercept power (IIP3), out-of-band (OB) IIP3, and input referred

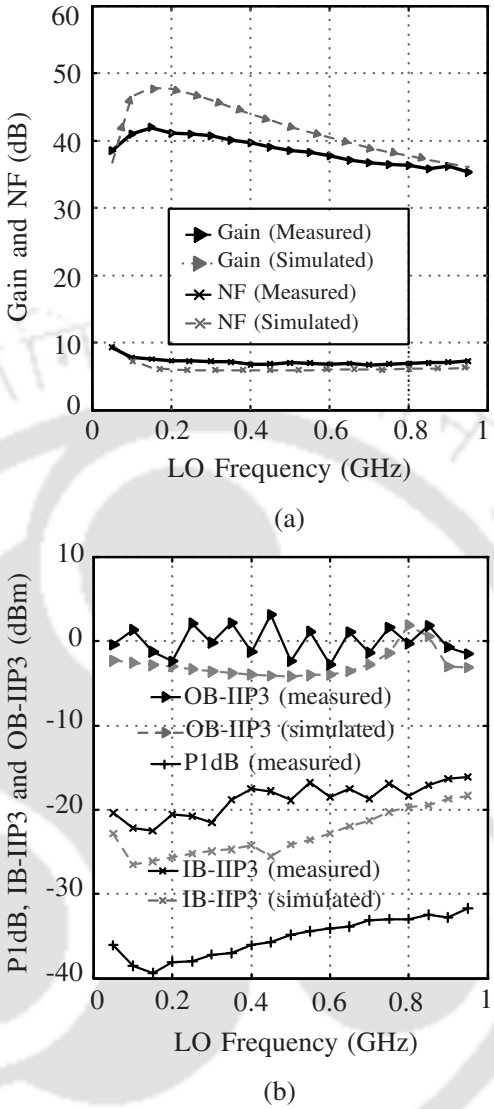


Figure 3.21: Measurement results in HD mode: (a) variation of gain and NF with LO frequency, and (b) variation of P1dB, IB-IIP3 and OB-IIP3 with LO frequency.

P1dB (P1dB) of the receiver. The spacing between the two tones for IB-IIP3 measurement is 2 MHz. For OB-IIP3 measurement, the two tones are chosen at $f_1 = f_{LO} - \Delta f$ and $f_1 = f_{LO} - 2\Delta f + 2$ MHz, where $\Delta f = 40$ MHz such that $\frac{\Delta f}{BW} = 5$. At 900 MHz, the receiver has an IB-IIP3 of ≈ -16 dBm and OB-IIP3 of ≈ -2 dBm. As discussed in Section 3.4.4, the linearity of this receiver is mainly limited by the HR stage. At 400 MHz, the receiver offers HR3 and HR5 of 20.3 dB and 24.2 dB respectively.

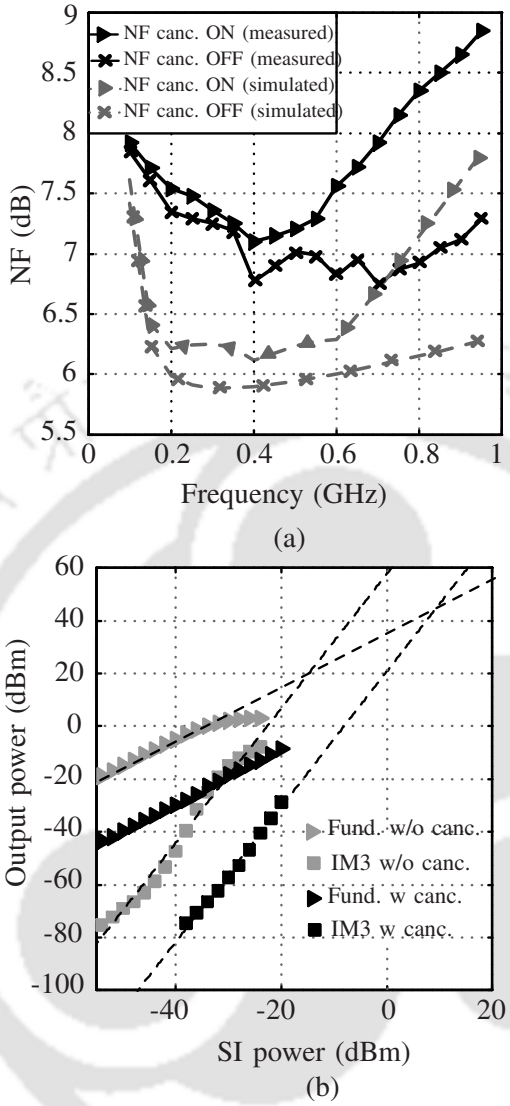


Figure 3.22: Measurement results in FD mode: (a) NF with the VM canceller ON and OFF, (b) fundamental and IM3 curves for IIP3 estimation.

3.6.2 When the SI canceller is ON

In FD mode, the receiver has an NF in the range of 7.1-8.8 dB which means a degradation of < 1 dB from the half-duplex mode. Fig. 3.22(a) shows the NF of the receiver when the VM is OFF and ON. Effective IB-IIP3 measurements are carried out using two in-band tones that are separated by 2 MHz at 900 MHz center. The power levels of the SI tones are swept from -60 to -20 dBm. Fig. 3.22(b) shows the fundamental and IM3 curves before and after the cancellation. The receiver has an effective IB-IIP3 of +7 dBm at 900 MHz. IB-IIP3 increased from -16 dBm in HD mode to

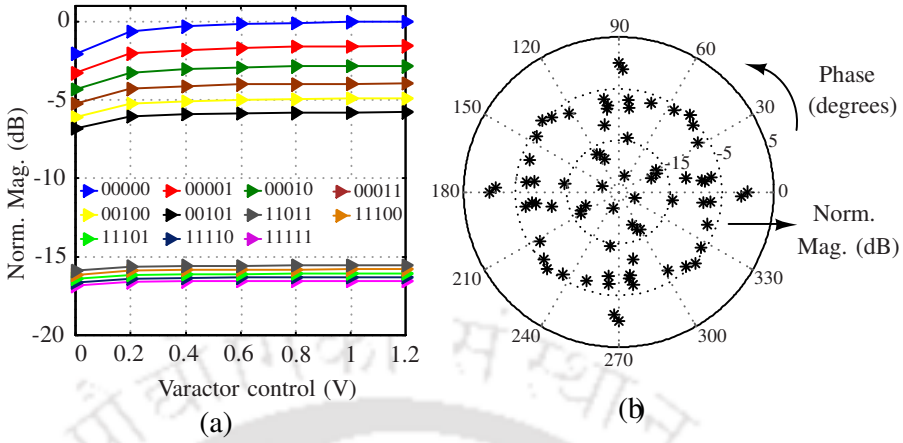


Figure 3.23: (a) Normalized output versus varactor tuning voltage, and (b) a few constellation points obtained in measurements.

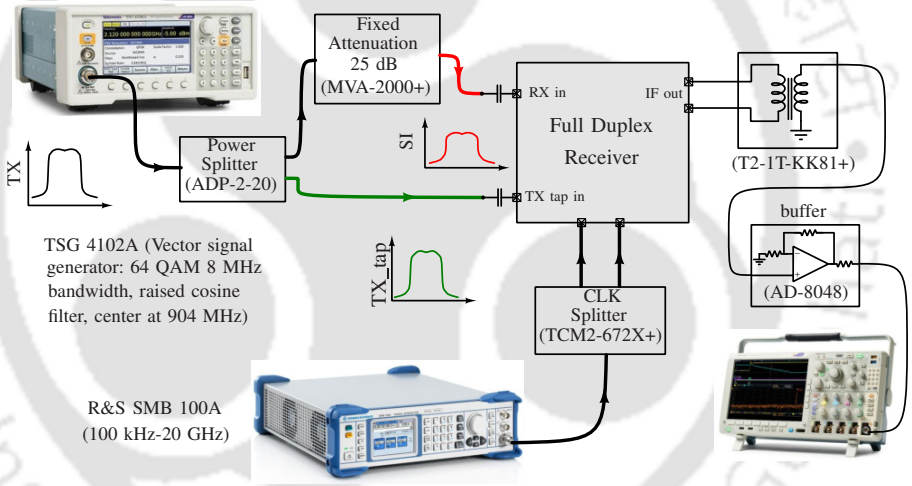


Figure 3.24: Measurement setup for FD mode.

+7 dBm in FD mode[3]. The maximum tolerable SI power for a given FD receiver is the power at which the IM3 components after the SI cancellation are equal to the noise floor. The maximum tolerable SI power for the current receiver is -27.5 dBm.

Fig. 3.23(a) shows variation of the output amplitude (normalized) with the varactor control voltage. Fig. 3.23(b) shows some of the constellation points obtained in measurements for various VM codes. The phase of the canceller signal is referenced to the output signal for equal I-code and Q-code. All instruments are synchronized with the same trigger signal. From Fig. 3.23(b), the proposed VM can cancel the SI in any of the four quadrants. The FD receiver is tested in the wired configuration

[3]In this measurement, varactors are not fine tuned

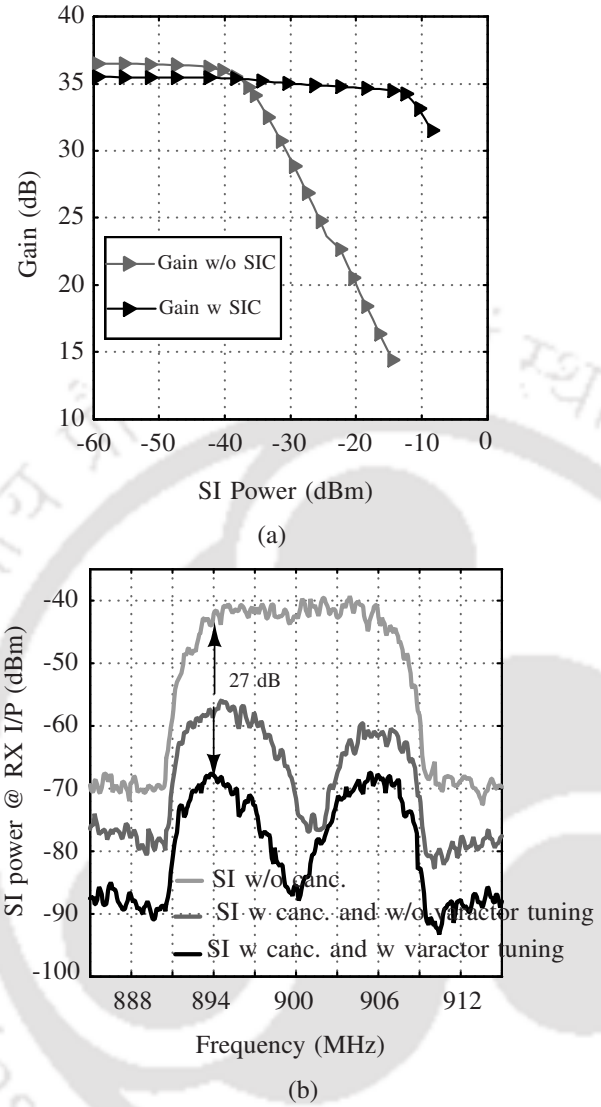


Figure 3.25: (a) Variation of receiver gain with SI power. (b) Spectrum of the 16 MHz signal at the receiver input before and after the SI cancellation with a GD of 1.2 ns

as shown in Fig. 3.24. The gain of the receiver is measured with respect to the desired signal in the presence of an SI. Fig. 3.25(a) shows variation of the receiver gain with SI power. In this measurement, the SI signal is kept at an offset of 200 kHz from the desired signal. The receiver has an input referred P1dB of -38 dBm (in the presence of SI) when the canceller is OFF and -14 dBm when the canceller is ON.

A 64-QAM signal with an 8 MHz bandwidth is used to test the cancellation in upper and lower sidebands around 900 MHz as shown in Fig. 3.24. The QAM signal is divided between the receiver and canceller ports using a power splitter (mini-circuits ADP-2-20). The SI spectrum cancellation is

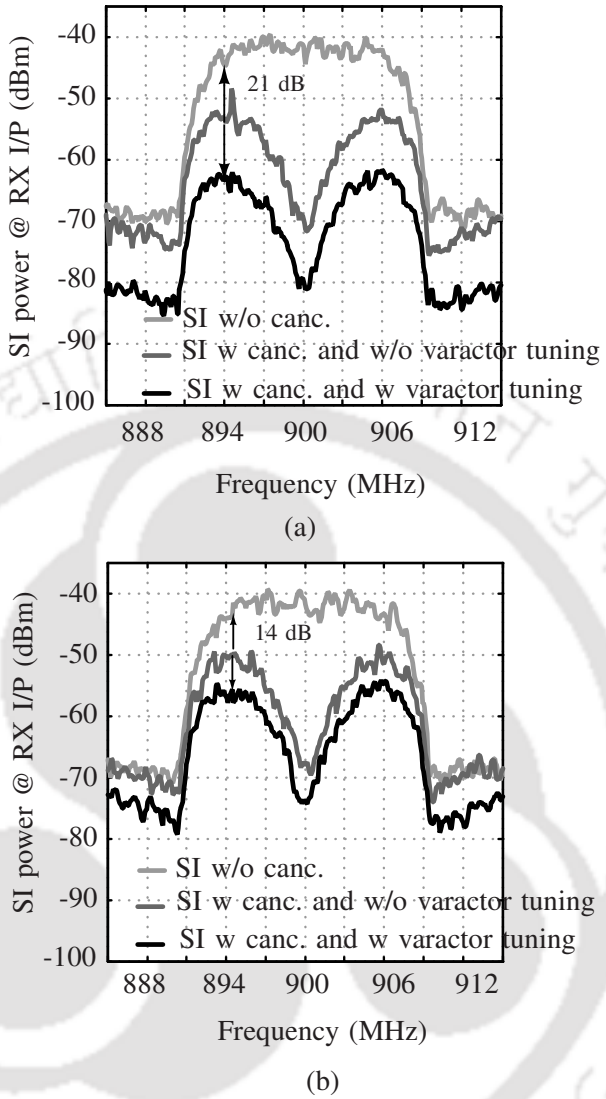


Figure 3.26: Spectrum of the 16 MHz signal at the receiver input before and after cancellation with GDs of (a) 2.2 ns and (b) 4.5 ns.

estimated for various group delays (GD) of the measurement cables (receiver and canceler inputs). Fig. 3.25(b) shows the spectrum of a 16 MHz SI signal before and after cancellation at the receiver input with a 1.2 ns GD. The receiver achieves $>$ 27 dB SIC in 15 MHz bandwidth at 1.2 ns group delay. The cancellation magnitude is further tested with higher group delay cables. Fig. 3.26(a) and 3.26(b) show the spectra of 16 MHz signals at the receiver input with 2.2 ns and 4.5 ns GDs respectively. From Fig. 3.26(a) and 3.26(b), as the GD increases the cancellation magnitude decreases for a given bandwidth.

At 900 MHz, the receiver consumes 17 mW of power. The eight-phase clock generator and the

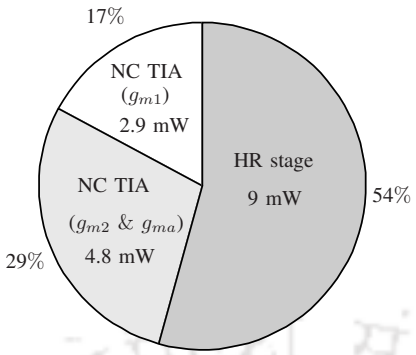


Figure 3.27: Analog power breakdown of the FD receiver

clock buffers consume 96 mW of power. Fig. 3.27 shows the breakdown of the analog power of the FD receiver. As discussed in Section 3.4.1 and 3.4.3, g_{m1}, g_{m2} and g_{ma} set the input match and NF of the receiver. The HR stage of the current FD receiver consumes 54% of the analog power. Any attempt to reduce the power consumption of the HR stage will have an impact on the linearity and bandwidth of the receiver. Table 3.1 shows the performance summary of the proposed IB-FD receiver and compares the measurement results with the prior art.

The proposed switched capacitor VM has less NF degradation in FD mode compared to the other FD receivers in Table 3.1. The IIP3 of the proposed receiver is at par with other receivers and could have been better if the overall gain has been reduced to 25 dB. One advantage of the continuously tunable VM, which has not been explored in this work, is the possibility of forming a feedback loop to automatically detect and cancel the SI. Automatic detection and cancellation of SI is still an open problem in FD radios. The VM presented in this work can provide the amplitude and phase tunability but not the delay tunability as required for an SI canceller. This lack of delay adjustment caused the poor cancellation of SI in the presence of large group delays as shown in Fig. 3.26. Integrated true-time delay cells such as the ones presented in [40,53–55] can be used in front of the proposed VM to realize a broadband SI canceller. The main challenge associated with true-time delays is delay-bandwidth product. Achieving large delay-bandwidth product is a serious concern. Moreover, tunable delays are required to cancel the multi-reflection echo signal. Though the proposed VM downmixer is mainly to cancel the transmitter echo in the receiving path, it can also cancel the transmitter leakage into the receiver. Transmitter leakage could be significant at mm-wave frequencies. The switched capacitor VM presented in this work uses a sampling circuit with very low time constant and hence is capable

Table 3.1: Comparison with other FD receivers

		ISSCC 2018 [32]	ISSCC 2017 [35]	JSSC 2018 [14]	JSSC 2015 [12]	JSSC 2015 [13]	This work
Architecture		Hybrid coupler based N-path circulator-RX	Circulator-RX+ On chip duplexer	Adaptive Double cancellation+RX	Wideband SIC based on FDE	Passive discrete VM+ Mixer first RX	Passive continuous VM+ Mixer first RX
Technology (nm)		65	65	40	65	65	130
Frequency Range (GHz)		0.55-0.9	0.61-0.975	1.7-2.2	0.8-1.4	0.15-3.5	0.1-0.95
Gain (dB)		15	28	20-36	27-42	24	42-37
DSB NF (dB)	RX	2.7	6.3	4-5	4.8	6.3	6.7-7.9
	FD	N/R	8	5.5-6.5	5.7-6.3	10-12.3	7.1-8.8
NF degradation (dB)		N/R	1.7	1.5	0.9-1.5	3.7-6	0.4-0.9
IIP3 (dBm)	RX	-4	-18.4	-5	-20	9/19	$-16^{\dagger}$
	Effective	$4^{\spadesuit}$	$9^{\spadesuit}$	17	2	21.5	$7^{\dagger}$
OOB IIP3 (dBm)		14	15.4	N/R	17	22	-2
Cancellation	Mag (dB)	$40^{\clubsuit}$	$40^{\clubsuit}$	$50^{\heartsuit,*}$	$20^{\ddagger}$	$15.6^{\star}$	$27^{\dagger,\diamond}$
	GD (ns)	N/R	N/R	N/R	9	4	1.2
	BW (MHz)	56	20	42	25	16	$15^{\square}$
SINDR (DB)		N/R	N/R	N/R	62.5 @ -30.7	71.4 @ -16.4	65.3 @ -27.5
Max SI/TX power (dBm)		$5.5^{\bigstar}$	$8^{\bigstar}$	$25^{\bigstar}$	$-16^{\blacksquare}/-8^{\sharp}$	$-16.4^{\triangledown}/1.5^{\blacksquare}$	$-27.5^{\triangledown}/-14^{\blacksquare}$
HR3/HR5 (dB)		N/R	N/R	N/R	N/R	N/R	$20.3/24.2^{\triangle}$
Power (mW)	RX	25	72	22	63-69	22-46	17
	Canc./Clock	24	36	11.5	44-182	1-10	$96^{\dagger}$
Active area (mm2)		$1^{\top}$	0.94	3.5	4.8	2	1.4
Frequency agile		No				Yes	
Which SIC		TX Leakage only		TX leakage and/or TX echo			

† at 900 MHz; ⋄ worst case cancellation in 15 MHz with group delay of 1.2 ns; □ -7.5 MHz to +7.5 MHz; △ at 900 MHz LO and uncalibrated; ♡ includes two-levels of cancellation; ∗ Measurement done with circulator ♠ with respect to TX power; ♣ TX leakage cancellation; ⊤ including pads; ⋆ worst case cancellation in 16 MHz from 2.5 GHz dipoles (group delay of 4 ns); ‡ worst case cancellation in 25 MHz from 1.4 GHz dipoles (group delay of 9 ns); ★ with respect to TX; ■ SI power at 1 dB RX gain compression; ∇ SI power at maximum SINDR; ♯ SI power for which cancellation is demonstrated

of working even at mm-wave frequencies provided the availability of the eight clock phases.

4

Linearity and NF Tradeoff in Input-Matched N-Path Mixer-First Receivers with Shunt-Feedback TIAs

Contents

4.1 Background

Chapter 3 shows that the proposed vector modulator is highly linear as it consists of passive switches and capacitors. Moreover, the vector modulator did not contribute much noise to the system. The IIP3 and NF of the system are mainly limited by the receiving path rather than the canceling path. To improve the performance of the proposed FD receiver, the baseband stage of the mixer-first receiver should have high IIP3 and have low NF. Therefore, the impact of baseband TIA on the linearity and NF of an N-path mixer-first receiver with an input match is studied in detail.

4.2 Introduction

N-path mixers offer tunable high-Q filtering at RF input due to their frequency translational property. This high-Q RF filtering of N-path mixers paves the way for SAW-less fully-integrated mixer-first receivers. The performance of N-path mixer-first receivers depends primarily on mixer switches and the baseband TIA topology. There are many studies on the analysis of the N-path mixer-first receivers [56–58]. [59] studies the impedance translational property in the passive mixer-first receivers and discusses the tradeoffs due to mixer non-idealities. [60] provides the optimum design choices for passive mixer-first receivers. [61] examines the NF limitations imposed by the TIA topology in mixer-first receivers with impedance matching.

In general, the linearity of a cascaded system is limited by the last gain stage of the cascade. Hence in a mixer-first receiver, TIA should be the linearity limiting factor. Similarly, gain and NF of the first amplifying block is crucial to suppress the noise due to the following blocks in a cascade. Since the TIA is the first amplifying block in a passive mixer-first receiver, the noise contribution of the TIA to overall noise is significant. This work studies the effect of a particular choice of TIA parameters, such as the feedback resistance value and the transconductance value of the OTA, on the overall noise and linearity performance of the N-path mixer-first receivers.

The rest of the paper is organized as follows. Section 4.3 reviews the input impedance of the N-path mixer-first receivers. Section 4.4 discusses the regimes of operation of mixer-first receivers. Section 4.5 presents the design examples and simulation results.

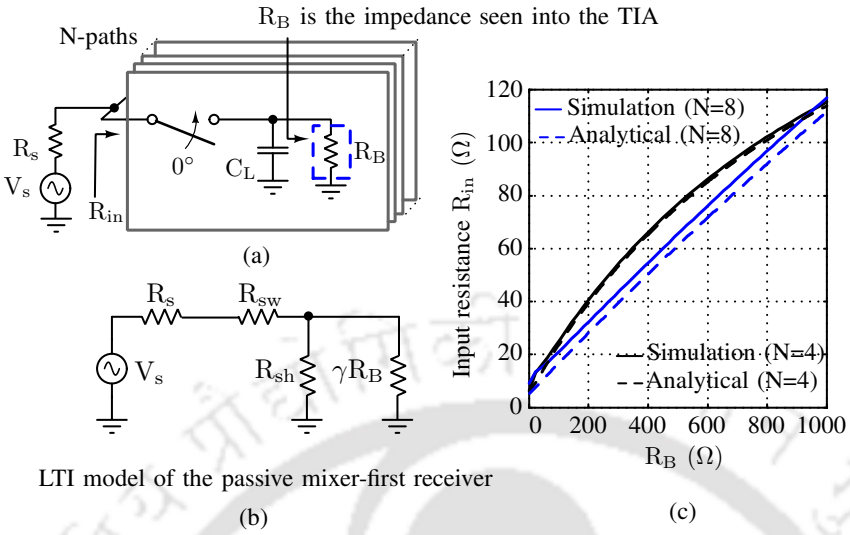


Figure 4.1: (a) N-path mixer-first receiver, and (b) its equivalent LTI model. (c) Verification of input impedance model for 4-path and 8-path mixer-first receivers.

4.3 Input impedance of a mixer-first receivers

Fig. 4.1(a) shows a typical N-path mixer-first receiver. In Fig. 4.1(a), R_B represents the impedance looking into the TIA input, R_s is the source resistance, C_L is the baseband shunt capacitor to suppress the high-frequency harmonics. Impedance translational properties of passive mixer-first receivers are studied in detail in [59], and proposed an equivalent LTI model as shown in Fig. 4.1(b). In the model shown in Fig. 4.1(b), R_{sw} is the ON-resistance of the switch, R_{sh} accounts for the power lost due to up-conversion of the input signal, and γ represents the mixer-topology (number of phases in N-path mixers) dependent constant.

The input resistance R_{in} of an N-path mixer-first receiver around the fundamental frequency is given by [59]

$$R_{in} = R_{sw} + \gamma R_B || R_{sh}, \tag{4.1}$$

where

$$\gamma = \begin{cases} \frac{2}{\pi^2} & \text{for N=4,} \\ \frac{2(2-\sqrt{2})}{\pi^2} & \text{for N=8,} \end{cases} \tag{4.2}$$

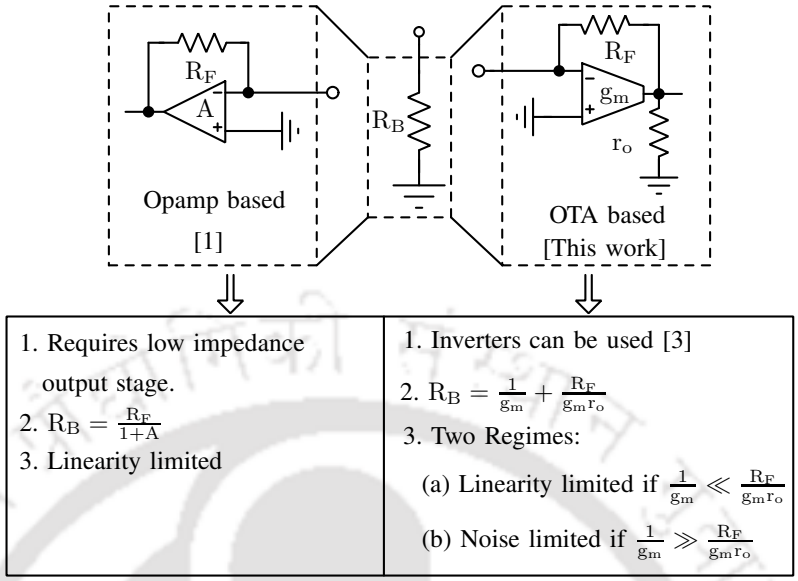


Figure 4.2: Comparison between Opamp based TIA and OTA based TIA.

and

$$R_{sh} = \begin{cases} (R_s + R_{sw})\frac{4\gamma}{1-4\gamma} & \text{for N=4,} \\ (R_s + R_{sw})\frac{8\gamma}{1-8\gamma} & \text{for N=8.} \end{cases} \tag{4.3}$$

The analytical expression in (4.1) is verified by the design and simulation of two N-path mixer-first receivers operating at $f_s = 1$ GHz. Ideal switches with 5 Ω ON-resistance and a resistance R_B are used in simulations. Fig. 4.1(c) shows the input resistance of 4-path and 8-path mixer-first receivers for different values of R_B. From Fig. 4.1(c), the R_B values should be close to 260 Ω and 370 Ω for N=4 and N=8 respectively for 50 Ω impedance matching.

4.4 Regimes of operation

From (4.1), R_B or the TIA input impedance plays a significant role in input matching. In passive mixer-first receivers, a shunt-feedback TIA is typically used [1]. The main amplifier in a shunt-feedback TIA can be an operational amplifier or an operational transconductance amplifier (OTA). These two TIA implementations are shown in Fig. 4.2. In [59], an opamp based TIA is considered[2]. An OTA based TIA is more frequently found in recent implementations of highly linear mixer-first receivers [56, 58,61,62]. In this work, a single stage OTA based TIA such as the one shown in Fig. 4.2 is considered.

[1] Other possibility is a common-gate amplifier based TIA.
[2] A detailed comparison between Opamp based TIA and OTA based TIA is discussed in Appendix A

In the OTA based TIA model shown in Fig. 4.2, R_F is the feedback resistance, g_m represents the transconductance of the main amplifier, and r_o represents the output impedance of the OTA. The input resistance of this OTA based TIA is given by

$$\begin{aligned} R_B &= \left[\frac{1}{R_F} - \frac{1}{R_F(r_o||R_F)} + \frac{g_m(r_o||R_F)}{R_F}\right]^{-1} \\ &\approx \frac{R_F}{g_m r_o||R_F} \approx \frac{1}{g_m} + \frac{R_F}{g_m r_o} \end{aligned} \tag{4.4}$$

The specific R_B value required for input matching can be realized either by using only $\frac{1}{g_m}$ or by using only $\frac{R_F}{g_m r_o}$ or by using both $\frac{1}{g_m}$ and $\frac{R_F}{g_m r_o}$. Based on this choice of g_m, the receiver operates in one of the two possible regimes. If we choose $r_o \gg R_F$ so that $R_B \approx \frac{1}{g_m}$, then the receiver operates in the noise-limited regime. In the noise-limited regime, the receiver exhibits poor NF but a relatively good IB-IIP3 which can be tuned by adjusting the R_F value. If we choose $\frac{1}{g_m} \ll \frac{R_F}{g_m r_o}$ so that $R_B \approx \frac{R_F}{g_m r_o}$, then the receiver operates in the linearity-limited regime. In the linearity-limited regime, the receiver exhibits poor IB-IIP3 but a relatively good NF which can be tuned by adjusting the g_m value.

4.4.1 Noise-limited regime

Fig. 4.3(a) shows an equivalent LTI model of the N-path mixer-first receiver for noise analysis. The main sources of noise in the model shown in Fig. 4.3(a) are switch resistance R_{sw}, shunt resistance R_{sh}, feedback-resistance R_F and noise of the OTA. Here the effect of r_o is neglected as $\frac{1}{g_m} \gg \frac{R_F}{g_m r_o}$. The noise factor of the receiver can be computed by calculating the noise contribution of each source at the output. The noise factor is given by

$$\begin{aligned} NF = 1 &+ \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left[\frac{R_a}{R_{sh}}\right]^2 + \frac{\gamma R_F}{R_s}\frac{1}{G_N^2} \\ &+ \gamma \overline{i^2}_{n,g_m}\left[\frac{R_F + \frac{R_p}{\gamma}}{1 - g_m R_F}\right]^2 \frac{1}{4KTR_s}, \end{aligned} \tag{4.5}$$

where, $R_a = R_s + R_{sw}$, $R_p = R_a||R_{sh}$, $\overline{i^2}_{n,g_m}$ is the noise current at the output of the OTA, and G_N is the transfer function of the receiver which is given by

$$\begin{aligned} G_N &= \left[\frac{1 - g_m R_F}{1 + \frac{g_m R_p}{\gamma}}\right]\left[\frac{R_{sh}}{R_{sh} + R_a}\right] \\ &\approx \left[\frac{1 - \frac{R_F}{R_B}}{1 + \frac{R_p}{\gamma R_B}}\right]\left[\frac{R_{sh}}{R_{sh} + R_a}\right] \text{ as } R_B \approx \frac{1}{g_m}. \end{aligned} \tag{4.6}$$

For amplification, we need $g_m R_F > 1$. The last two terms of (4.5) represent the noise contribution

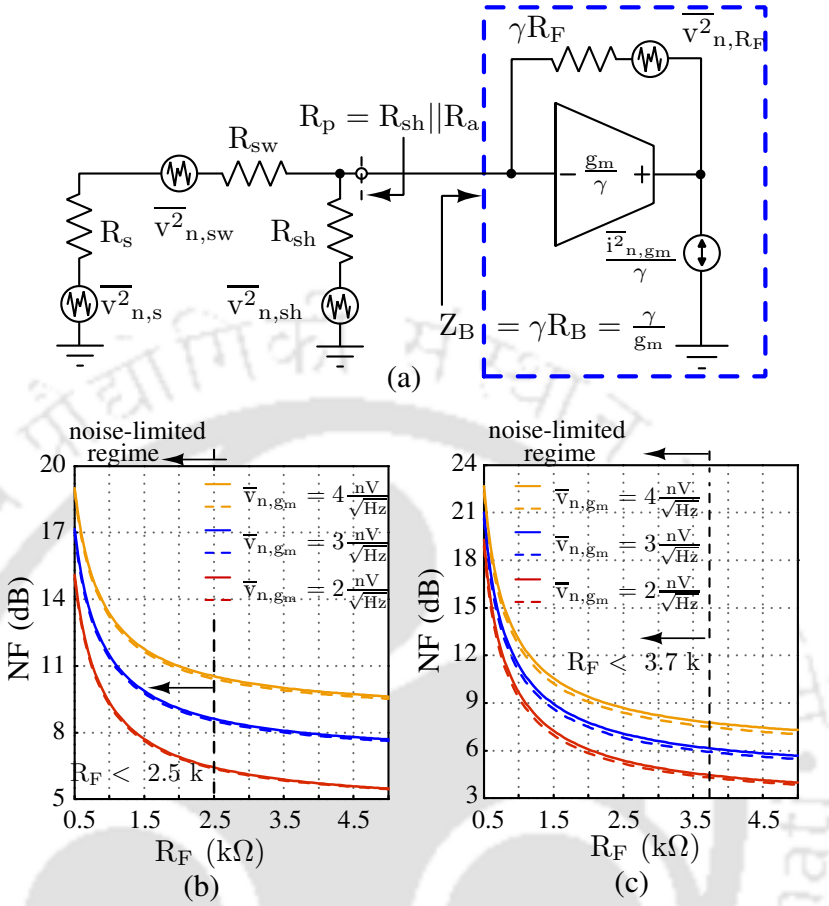


Figure 4.3: (a) Equivalent LTI model of the receiver for noise analysis in the noise-limited regime. Variation of NF with R_F for different input referred noise voltage of transconductor (b) in a 4-path mixer-first receiver, and (c) in an 8-path mixer-first receiver (Solid lines indicate simulation, while dashed lines indicate (4.5)).

of the TIA to the overall receiver noise. (4.5) is verified by the design and simulation of 4-path and 8-path mixer-first receivers. Ideal switches with 5 Ω ON-resistance, and a VCCS with an appropriate input referred noise voltage $\overline{v^2}_{n,g_m} = \frac{\overline{i^2}_{n,g_m}}{g_m^2}$ to model the OTA are used in simulations. Moreover, the OTA is assumed to have $g_m r_o = 100$ [3]. Fig. 4.3(b) and Fig. 4.3(c) show the variation of NF with feedback resistance R_F for different $\overline{v^2}_{n,g_m}$ in 4-path and 8-path receivers respectively. The NF of the receiver in this noise limited regime depends on $\overline{v^2}_{n,g_m}$ and R_F. The g_m required for input matching is ≈ 4 m℧ in a 4-path receiver and is ≈ 2.7 m℧ in an 8-path receiver. The noise-limited regime in the plots shown in Fig. 4.3 is separated by a dashed line where $\frac{1}{g_m}$ is 10 times more than $\frac{R_F}{g_m r_o}$.

[3] In this work, a single stage OTA is considered where $g_m r_o$ is a constant. A two-stage OTA restricts the receiver to the linearity-limited regime only. [56, 58, 61, 62] use single stage OTAs.

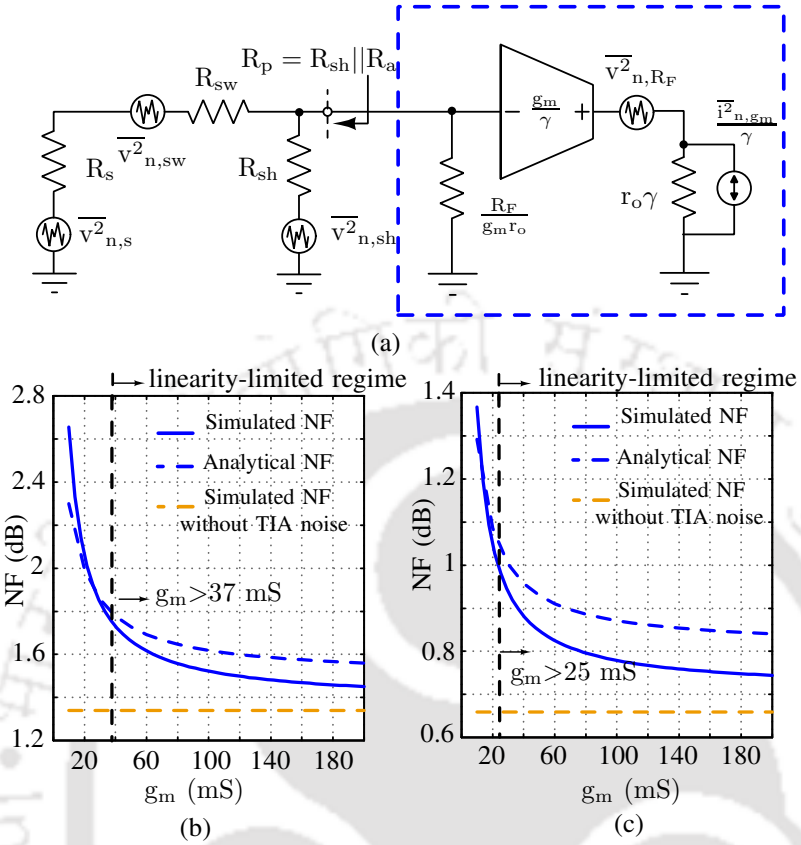


Figure 4.4: (a) Equivalent LTI model of the receiver for noise analysis in the linearity-limited regime. Variation of NF with g_m with and without TIA noise (b) in a 4-path mixer-first receiver, and (c) in a 8-path mixer-first receiver (Solid lines indicate simulation, while dashed lines indicate (4.7)).

4.4.2 Linearity limited regime

A noise equivalent LTI model of the receiver under study is shown in Fig. 4.4(a). Using Miller theorem, the feedback resistor R_F can be modeled by resistive terminations at the input and output of the OTA. Since $R_F \gg r_o$, only r_o is shown at the output of the OTA in Fig. 4.4(a). The noise voltage due to R_F is added to the OTA output. From Fig. 4.4(a), the noise factor can be computed as

$$\begin{aligned} NF = 1 + \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left[\frac{R_a}{R_{sh}}\right]^2 + \frac{\gamma R_F}{R_s}\frac{1}{G_L^2} \\ + \frac{\gamma \overline{i^2}_{n,g_m} r_o^2}{G_L^2}\frac{1}{4KTR_s}, \end{aligned} \tag{4.7}$$

$$\begin{aligned} \text{where } G_L &= \left[\frac{\gamma g_m r_o R_{sh} R_F}{\gamma R_F R_{sh} + \gamma R_a R_F + g_m r_o R_{sh} R_a}\right] \\ &\approx \left[\frac{g_m r_o}{1 + \frac{R_a}{R_{sh}} + \frac{R_a}{\gamma R_B}}\right] \text{ as } R_B \approx \frac{R_F}{g_m r_o}. \end{aligned} \tag{4.8}$$

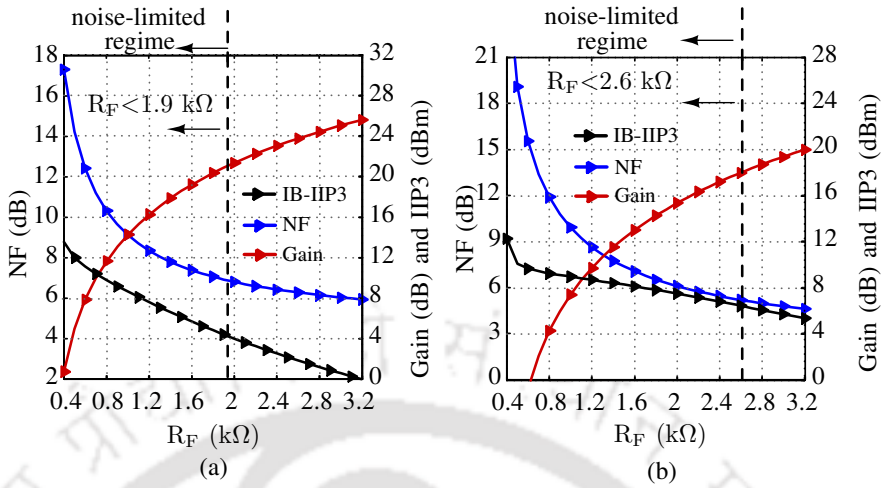


Figure 4.5: Variation of NF, gain and IB-IIP3 of the receiver (implemented with inverter based TIA) with feedback resistance R_F in (a) a 4-path mixer-first receiver, and (b) in an 8-path mixer-first receiver.

Using $R_{sh} \gg R_a$ from (4.3), the above expression can be further simplified to

$$G_L \approx \left[\frac{g_m r_o}{1+\frac{R_a}{\gamma R_B}}\right]. \tag{4.9}$$

(4.7) is verified by the design and simulation of 4-path and 8-path mixer-first receivers. Ideal switches with 5 Ω ON-resistance, and a VCCS to model the OTA are used in the simulations. The noise current of an OTA depends on the g_m value. For simulation and verification purposes, $\overline{i^2}_{n,g_m}$ is assumed to be equal to $4KT\gamma_M g_m$, where $\gamma_M \approx \frac{2}{3}$ is the noise proportionality constant. Fig. 4.4(b) and Fig. 4.4(c) show the variation of NF with the g_m value in 4-path and 8-path mixer-first receivers respectively. The R_F required for input matching in a 4-path, and an 8-path mixer-first receivers respectively are 27 kΩ and 39 kΩ. The linearity-limited regime is separated in the plots of Fig. 4.4 by a dashed line where $\frac{1}{g_m}$ is 10 times less than $\frac{R_F}{g_m r_o}$. From Fig. 4.4(b) and Fig. 4.4(c), one can infer that the NF of the receiver in a linearity-limited regime can be brought closer to the NF of the mixer alone. The cost of reducing the NF is the increase in power consumption to increase the g_m value. By substituting γ, R_{sh} and R_B values from (4.2) and (4.3) in (4.6) and (4.9), one can deduce that $G_N \ll G_L$. For a given output swing, a system with lower gain will support higher input amplitude and hence will have higher IB-IIP3. Thus, the IB-IIP3 of a receiver operating in the linearity-limited regime is smaller than the IB-IIP3 of a receiver operating in the noise-limited regime.

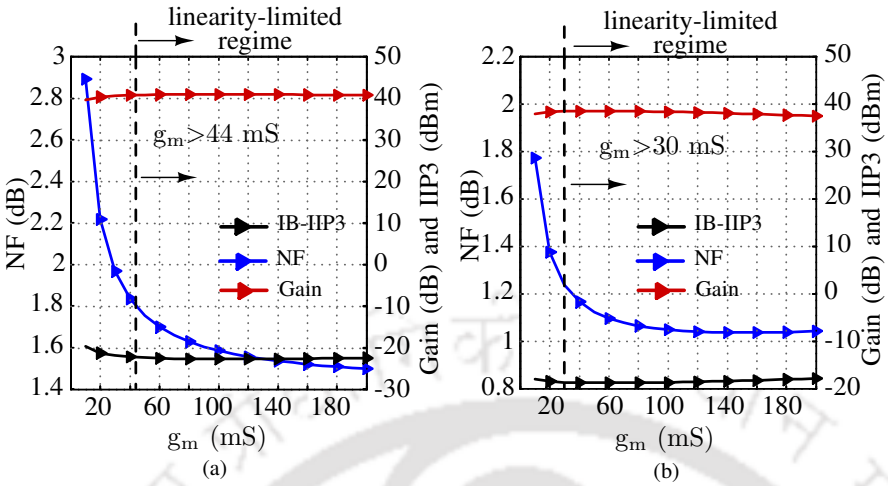


Figure 4.6: variation of NF, gain and IB-IIP3 of receiver (implemented with inverter based TIA) with transconductance g_m in (a) a 4-path mixer-first receiver, and (b) in an 8-path mixer-first receiver

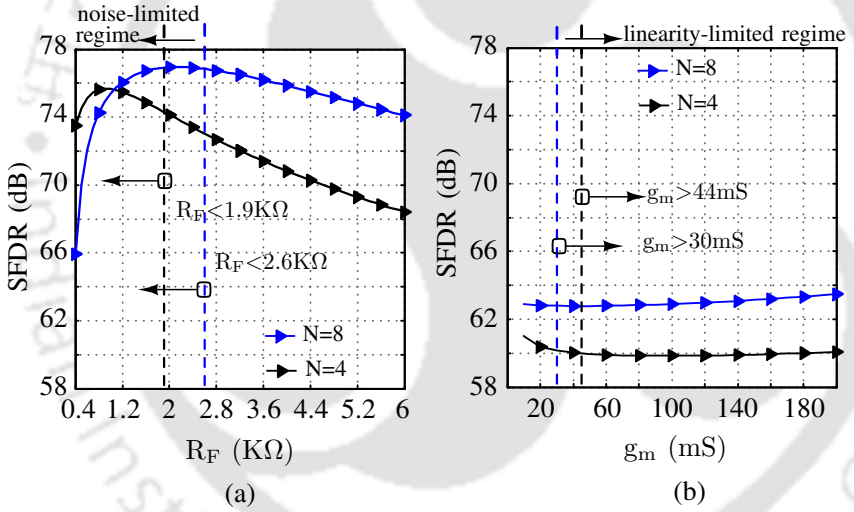


Figure 4.7: (a) variation of SFDR of a 4-path and a 8-path mixer-first receiver (implemented with inverter based TIA) with R_F, (b) variation of SFDR of 4-path and 8-path mixer-first receiver (implemented with inverter based TIA) with g_m

4.5 Design Examples and simulation results

A 4-path and an 8-path mixer-first receivers are designed in a CMOS 65nm technology. A supply voltage of 1.2 V is used. The switches are implemented using NMOS transistors with $\frac{W}{L} = \frac{128\ um}{60\ nm}$ to have an ON-resistance of 5 Ω. To ensure that the linearity is not limited by the switches, the gates of NMOS switches are ac coupled and separate biasing is provided. Ideal non-overlapping clocks are used in these simulations. A pseudo-differential inverter based OTA is used to implement the TIA. A channel length of 1 μm is used for PMOS and NMOS transistors in the OTA to reduce the effect

Table 4.1: Performance summary of N-path mixer-first receivers

Specification/ Parameters	Noise-limited regime		Linearity -limited regime	
	N=4	N=8	N=4	N=8
Parameters for input match†	g_m=4	g_m=2.7	R_F=16	R_F=24
Design condition†	R_F<1.9	R_F<2.6	g_m>44	g_m>30
NF (dB)	>6.9	>5.1	<1.8	<1.2
IB-IIP3‡ (dBm)	>4	>6	≈-22	≈-19
Gain (dB)	<22	<20	≈41	≈39
SFDR (dB)*	73-77	66-77	≈ 63	≈ 60
Power (mW)	1.05	1.48	>11.43	>15.24

† units of g_m and R_F are mS and kΩ respectively.
‡ Spacing between the two tones is 1 MHz.
* SFDR = $\frac{2(IIP3+174-NF-10\log B)}{3}$, where B=1 MHz.

of flicker noise and channel length modulation on the simulation results. The intrinsic gain of each inverter is found to be 70. For higher g_m values, multiple inverters are used in parallel.

4.5.1 Noise-limited regime

Fig. 4.5(a) and Fig. 4.5(b) show the variation of simulated NF, gain and IB-IIP3 with R_F in the 4-path and 8-path mixer-first receivers respectively. From Fig. 4.5(a) and Fig. 4.5(b), the best possible NF is 6.9 dB in the 4-path mixer-first receiver and 5.1 dB in the 8-path mixer-first receiver. The IB-IIP3 at the edge of the noise-limited regime is ≈ 4 dBm. From Fig. 4.5, one can also observe that the gain and IIP3 values can be adjusted by varying the R_F value in the noise-limited regime. The dc power consumption of the 4-path receiver is 1.05 mW, and the 8-path receiver is 1.48 mW.

4.5.2 Linearity-limited regime

Fig. 4.6(a) and Fig. 4.6(b) show the variation of simulated NF, gain and IB-IIP3 with the g_m value in the 4-path and 8-path receivers respectively. In this regime, the NF of the 4-path receiver is less than 1.8 dB and the NF of the 4-path receiver is less than 1.2 dB. The large R_F required for the input matching degrades the overall linearity of the receiver. From Fig. 4.6(a) and Fig. 4.6(b), the IB-IIP3 at the edge of the linearity-limited regime is ≈ -22 dBm in the 4-path receiver and -19 dBm in the

8-path receiver. The 4-path receiver has a gain of 41 dB and the 8-path receiver has a gain of 39 dB. In the linearity-limited regime, the noise contribution of the OTA can be reduced by increasing the g_m value. Increasing g_m will increase the dc power consumption of the receiver. The power consumption of a receiver operating in the linearity-limited regime is higher than a receiver operating in the noise-limited regime.

4.5.3 Design for high SFDR

Fig. 4.7(a) and Fig. 4.7(b) show the SFDR variation in 4-path and 8-path mixer-first receivers in the two regimes that we have discussed. From Fig. 4.7(a), one should design an N-path mixer-first receiver to operate at the edge of the noise-limited regime to achieve the best possible SFDR with input matching. In the linearity limited regime, SFDR is relatively independent of the OTA gain. Another observation from Fig. 4.7(a) and Fig. 4.7(b) is that an 8-path mixer-first receiver will have higher SFDR than a 4-path mixer-first receiver. The performance of the N-path mixer-first receivers in the two regimes of operation is summarized in Table. 4.1.

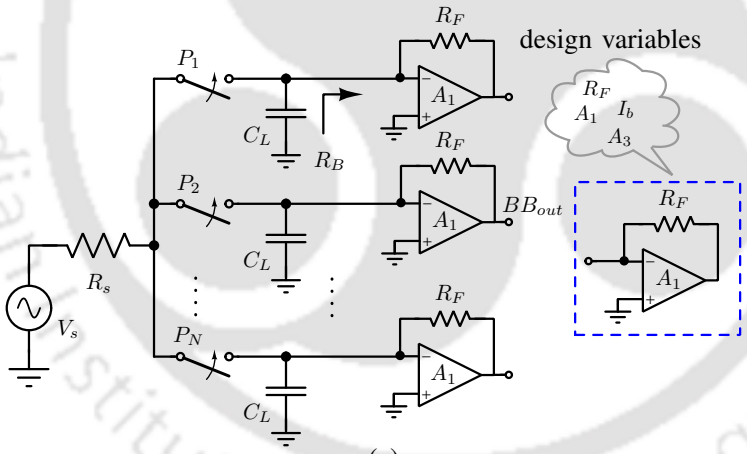
5

A Mixer-First Receiver With Second-Order Baseband Noise-canceling TIA

Contents

5.1 Motivation

The next-generation cellular systems require frequency tunable narrow-band receivers, which can operate up to 6 GHz [63]. Moreover, these receivers need to tolerate large IB [64] and OB [65] blockers due to several wireless standards in the sub-6 GHz range. Typical OB-IIP3 requirement for an LTE receiver can be as high as +35 dBm [66]. Fully integrated transceivers with only a single antenna for transmission and reception require an antenna interface module such as a duplexer [67] or a circulator [35]. The loss in these antenna interface modules limits the NF of the receiver. In battery-operated wireless systems such as mobile phones, the power consumption of the receiver affects the battery lifetime. A low power receiver enhances the battery lifetime. From these requirements, a next-generation radio receiver should have the following characteristics: frequency agility, close-in blocker tolerance, low NF, low power consumption, and input-match. It may not be possible to tradeoff one of these specifications for the sake of another. Passive mixer-first receivers offer all the characteristics



(a)

Specification	Constraint on opamp
1. Input-match	$A_1 = \frac{R_F}{R_B} - 1$
2. High IB-IIP3	Low A_3
3. High OB-IIP3	Low A_3
4. Low NF	Low $\overline{v_{n,A}}$
5. Low Power	Low I_b

(b)

Figure 5.1: (a) Typical N-path mixer-first receiver with a shunt feedback TIA. (b) Design constraints on the opamp to achieve required specifications.

that are required for next-generation cellular systems. There are many recent efforts to improve

the performance of passive mixer-first receivers further. [68–72] proposed different techniques in baseband TIAs to enhance the channel selectivity and blocker resilience. [73] proposed a bottom-plate mixing technique to improve the OB-IIP3 by reducing the gate-source voltage modulation of MOSFET switches. [74] demonstrated a low power mixer-first receiver for wireless sensor networks. [75–77] achieved low NF by canceling the noise of the matching device in the mixer-first receiver. In the works [68–71, 73–77], some of the specifications are improved at the expense of others.

The main objective of this work is to design an N-path mixer-first receiver with independently tunable performance metrics. In order to understand the challenges in this design, we need to revise the performance tradeoffs in a typical mixer-first receiver [78]. Fig. 5.1(a) shows an N-path mixer-first receiver with a shunt feedback TIA. In Fig. 5.1(a), C_L is the shunt capacitor at the input of the TIA, R_s is the source resistance, and R_{sw} is the on-resistance of mixer switches. The design of a mixer-first receiver involves choosing appropriate values for the feedback resistor (R_F), the open-loop gain of the opamp (A_1) and the biasing current of the opamp (I_b). The effect of mixer switches on the performance of a passive mixer-first receiver is analyzed in [52], and an optimal design strategy is presented in [79]. The analyses in [52] and [79] assumes an ideal opamp in the baseband with a high gain and no non-linearity. From the linearity analysis presented in [52, 79] and the receiver implementations presented in [75, 80–82], it can be said that the passive mixers are more linear than the TIAs used in mixer-first receivers. Therefore, in a practical design, the TIA limits the performance of the receiver more often than the mixer switches. In the following discussion, the switches are assumed to be highly linear, and the opamp is assumed to have a third-order non-linearity. Let the opamp has the following transfer characteristics.

$$v_{out} = A_1 v_{in} + A_3 v_{in}^3, \tag{5.1}$$

where v_{out} is the output voltage, v_{in} is the input differential voltage, and A_3 is the third-order polynomial coefficient of the output voltage.

The input resistance of the N-path mixer-first receiver at the center frequency is given by [52]

$$R_{in} = R_{sw} + \left(R_{sh} || \gamma \left[\frac{R_F}{1 + A_1} \right] \right), \tag{5.2}$$

where R_{sh} accounts for the power loss due to the up-conversion of the input signal, and γ represents a constant that depends on the number of paths. From (5.2), the open-loop gain of the opamp required

for the input-match is given by

$$A_1 = \frac{R_F}{R_B} - 1, \tag{5.3}$$

$$\text{where } R_B = \frac{1}{\gamma}\frac{(R_{sh}R_s - R_{sw}R_{sh})}{(R_{sw} + R_{sh} - R_s)}. \tag{5.4}$$

In a practical implementation, a programmable resistor is often used for R_F to overcome the impedance variations. The R_F value is set based on the following expression to achieve the RF input match.

$$R_F = (1 + A_1)R_B. \tag{5.5}$$

The IB-IIP3 and OB-IIP3 of the receiver in Fig. 5.1(a) are given below.[1]

$$\text{IB} - \text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{A_1}{A_3}\right|\left[1 + \frac{R_{Th}}{\gamma R_B}\right]^3}.\frac{R_a}{R_{Th}}, \tag{5.6}$$

and

$$\text{OB} - \text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{A_1}{A_3}\right|\left[\frac{\left(1 + \frac{R_{Th}}{\gamma R_B}\right)^2 + \left(\frac{\Delta\omega}{\omega_o}\right)^2}{1 + \left(\frac{\Delta\omega}{\omega_o}\right)^2}\right]^{\frac{3}{2}}} \times \frac{R_a}{R_{Th}}.\sqrt{1 + \left(\frac{\Delta\omega}{\omega_o}\right)^2}, \tag{5.7}$$

where $R_a = R_s + R_{sw}$, $R_{Th} = R_{sh}||R_a$, $\omega_o = \frac{\gamma}{R_{Th}C_L}$, and $\Delta\omega$ is the offset from the center frequency. From the above expressions, the IIP3 of the receiver is limited by the opamp third-order linearity coefficient (A_3).

Similarly, the noise factor of the receiver is given by [52]

$$\text{NF} = 1 + \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left[\frac{R_a}{R_{sh}}\right]^2 + \gamma\frac{R_F}{R_s}\left[\frac{R_a}{\gamma R_F}\right]^2 + \gamma\frac{\overline{v_{n,A}^2}}{4KTR_s}\left[\frac{R_a}{\gamma R_F} + \frac{R_a + R_{sh}}{R_{sh}}\right]^2, \tag{5.8}$$

where $\overline{v_{n,A}}$ is the input noise voltage of the opamp. The input noise voltage of the opamp is inversely proportional to the biasing current. The noise of the opamp can be minimized by biasing it with a large current [52]. The static power consumption of the receiver depends on the opamp biasing current I_b and is given by

$$\text{Power} = V_{op}I_b, \tag{5.9}$$

where V_{op} is the opamp supply voltage. From (5.3)-(5.9), the following opamp design constraints can be deduced for the N-path mixer-first receiver shown in Fig. 5.1(a).

- The input-matching of the receiver requires an opamp with a gain equal to (5.3).

[1]The IB-IIP3 and OB-IIP3 expressions are derived and validated in Appendix B.

- For a high linearity receiver, we need an opamp with a low third-order polynomial coefficient (A_3).
- To achieve a low NF for the receiver, an opamp with low input noise voltage ($\overline{v_{n,A}}$) is required.
- Low power consumption requires an opamp with low bias current.

Fig. 5.1(b) summarizes the above constraints in a tabular form. To design a single opamp with all the above requirements, we need to break the fundamental tradeoffs in analog circuit design [83]. To avoid the need for such a 'golden' opamp, this work proposes a second-order baseband noise cancellation scheme that breaks the performance tradeoffs in a mixer-first receiver. In mixer-first receivers, the baseband noise cancellation scheme was previously reported in [33, 84, 85]. The receivers in [33, 84, 85] used a first-order baseband noise cancellation scheme. Each of these receivers is designed for a specific application such as for full-duplex radios in [33, 84], and for base-station applications with large IF bandwidth in [85]. The IF bandwidth of the receiver in [85] is limited by the opamp compensation scheme rather than the shunt capacitance at the mixer output. This affected the OB-IIP3 of the receiver in [85] at close-in offset frequencies ($BW < \Delta f < 4 \times BW$). The focus of this work is mainly on the optimal design of mixer-first receivers including the TIA performance into consideration. A step-by-step design procedure is also discussed in the latter part of this work. Using the proposed second-order BB noise-canceling TIA, this work also reports a CMOS mixer-first receiver that achieved the best IB and close-in OB Figure-of-Merits (FOMs) among the state-of-the-art mixer-first receivers. The rest of the chapter is organized as follows. Section 5.2 presents the various N-path mixer-first receivers for enhanced linearity. Section 5.3 presents the Section 5.3 describes the baseband TIA. Section 5.4 provides the receiver analysis. Section 5.5 describes the brief design procedure and the implementation details of the proposed receiver. Measurement results are presented in Section 5.6.

5.2 Review of N-path mixer-first receivers for enhanced linearity

In this section, we present the various N-path mixer-first receivers for enhanced linearity and low NF.

5.2.1 Mixer-first receiver with baseband noise-canceling circuit [85]

[85] propose a baseband noise-canceling receiver to increase IB linearity with a low NF. It is a noise-canceling architecture, where all active circuits work at baseband frequencies. Fig. 5.2 shows

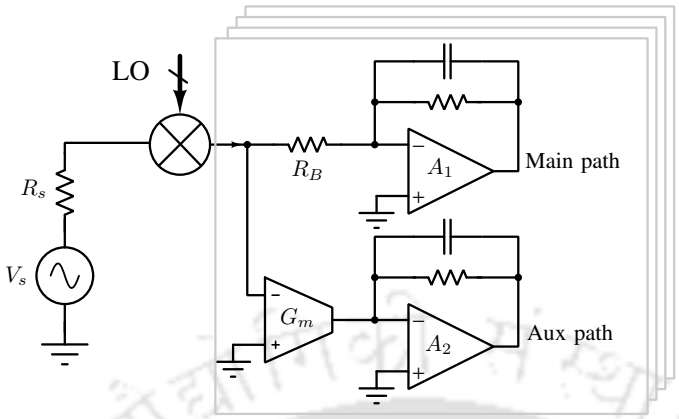


Figure 5.2: Mixer-first receiver with baseband noise-canceling circuit [85].

the mixer-first receiver with baseband noise-canceling TIA. To achieve the input match, resistor R_B is used whose impedance is frequency translated to the input by the passive mixer. The baseband circuit consists of an auxiliary path having a low noise transconductor (LNTA) stage G_m. LNTA cancels the noise of the resistor R_B. The baseband circuit is designed for a wide bandwidth in the mixer-first receiver. Therefore, the TIA opamp is implemented with only inverters as gain stages. The inverter stages avoid unnecessary internal nodes so that a high bandwidth can be achieved. Moreover, there are also other advantages due to the current reuse technique and rail-to-rail output swing. The main path gives sufficient gain to 175 MHz to achieve the required linearity.

Measured results show an IB-IIP3 of $\geq$ 9 dBm for a baseband bandwidth of 175 MHz with sub-5 dB NF across 1-6 GHz. The receiver achieves good specification because all active circuits operate in baseband and can be designed using feedback, both the LNTA and the TIA. Due to the noise-canceling properties, the tradeoff between the input match and the NF is broken.

5.2.2 Mixer-first receiver driving an impedance with 40 dB/decade roll-off [72]

A second-order passive mixer-first receiver is presented in [72] to improve channel selectivity, linearity, and noise figure in the presence of OB blockers. An impedance rolls off at 40 dB/decade is used as the load to an N-path filter. The synthesis of the load is started from the required impedance transfer function to its actual circuit realization. Fig. 5.3 shows the mixer-first receiver driving an impedance with a 40 dB/decade roll-off. The load at the output of the mixer is a series combination of C_1 and Z_1. Here, Z_1 can be realized using a parallel combination of a negative resistance (-R_1) and a negative capacitance (C_1). The impedance load offers a 40 dB/decade roll-off and gives the

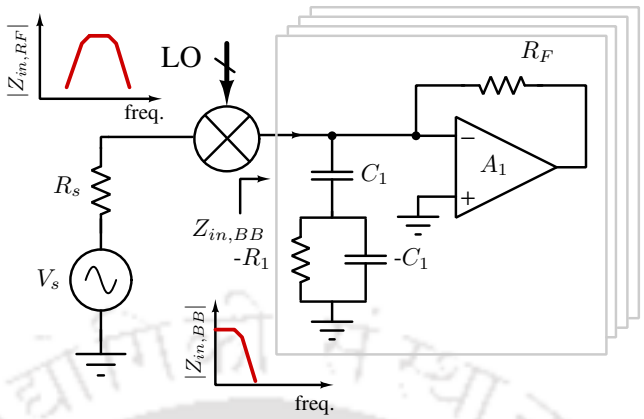


Figure 5.3: Mixer-first receiver driving an impedance with 40 dB/decade roll-off [72].

desired higher-order filtering at RF. The receiver is capable of broadband operation from 0.2-2 GHz. It achieves an OB-IIP3 of +33 dBm and a blocker P1dB of +12 dBm. It achieves an NF of 4.4 dB with less than 2 dB degradation in NF for a 0 dBm blocker.

5.2.3 Mixer-first receiver with baseband capacitive positive feedback [65]

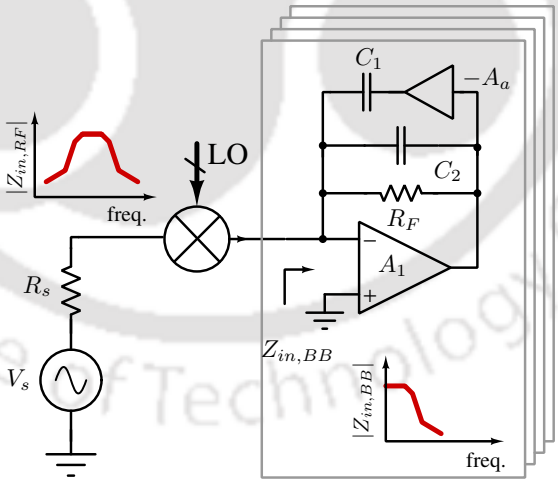


Figure 5.4: Mixer-first receiver with baseband capacitive positive feedback [65].

A mixer-first receiver enhanced with capacitive positive feedback is presented in [65] to obtain a steeper filter roll-off and enhanced linearity while keeping low NF. The capacitive negative feedback across the baseband amplifier serves as a blocker bypassing path, while an extra capacitive positive feedback path offers further blocker rejection. Fig. 5.4 shows the mixer-first receiver with baseband capacitive positive feedback. The combination of the new positive feedback path C_2 and the conven-

tional negative feedback path C_1 synthesizes two complex poles resulting in a theoretical 4th order RF bandpass and 2nd order baseband low pass filtering. The quality factor Q is adjustable by changing the ratio of C_1 and C_2. It should be noted that both baseband capacitive feedback paths can have high linearity as well as low noise. It covers all sub-6 GHz cellular bands and achieves a high IIP3 of +39 dBm and blocker 1 dB gain compression point of +12 dBm for a blocker frequency-offset of 80 MHz at LO frequency of 2 GHz. The NF ranges from 2.4 dB at LO frequency of 1 GHz to 5.4 dB at LO frequency of 6 GHz. The measured desensitization is only 2.2 dB for 0 dBm blocker and 7.1 dB for 8 dBm blocker, demonstrating robustness to transmitter leakage and strong blockers.

5.2.4 Mixer-first receiver with baseband shunt notch [69]

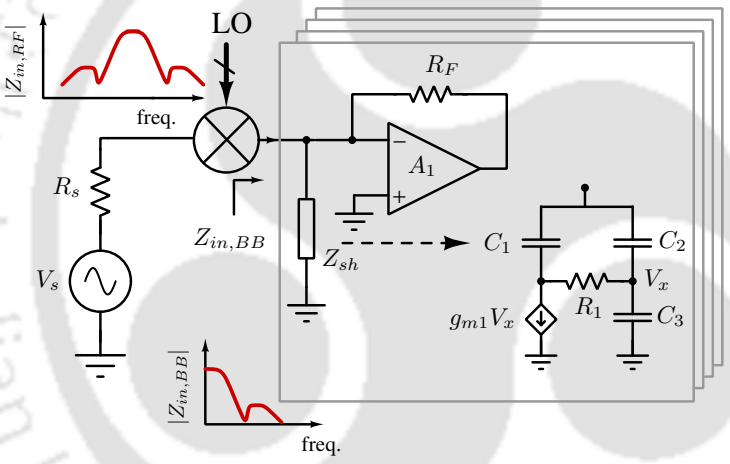


Figure 5.5: Mixer-first receiver with baseband shunt notch [69].

Shunting notch provides steeper baseband, and impedance roll-off and improved adjacent-channel linearity. The shunting notch topology configures the input impedance to have a pair of complex poles, followed by a notch from a pair of complex zeros, followed by a wider real pole. Fig. 5.5 shows the mixer-first receiver with baseband shunt notch. The positive feedback pole is disconnected in this mode; thus, the baseband amplifier only has a negative feedback resistor for matching the antenna impedance. In the shunting circuit g_{m1}, R_1, and C_2 form a structure similar to an active inductor, which acts in series with C_1 to form the notch. C_2 band-limits the LC shunt to prevent the circuit from generating a high impedance parallel resonance beyond the desired cutoff frequency due to the parasitic shunting capacitance. C_3 sets the real pole and is selected, such that $C_3 << C_2$. Beyond the complex conjugate zeros, the filter shape flattens off to a level OB resistance. Therefore, gm is

selected, so that dominant impedance is set by the on-resistance of the mixer switches. Again, Q can be tuned to flatten the IB response, sharpen the corner, and counter-act roll-off from the complex zeros. The receiver operates at RF frequencies from 2-11 GHz and achieves a blocker P1dB compression of 1.8 dBm and IIP3 of +20 dBm for a blocker frequency-offset of 70 MHz (bandwidth=30 MHz) at LO frequency of 5 GHz. The NF ranges from 9±1 dB to 11±1 dB over the frequency range of LO frequency of 2-8 GHz.

5.3 Baseband TIA

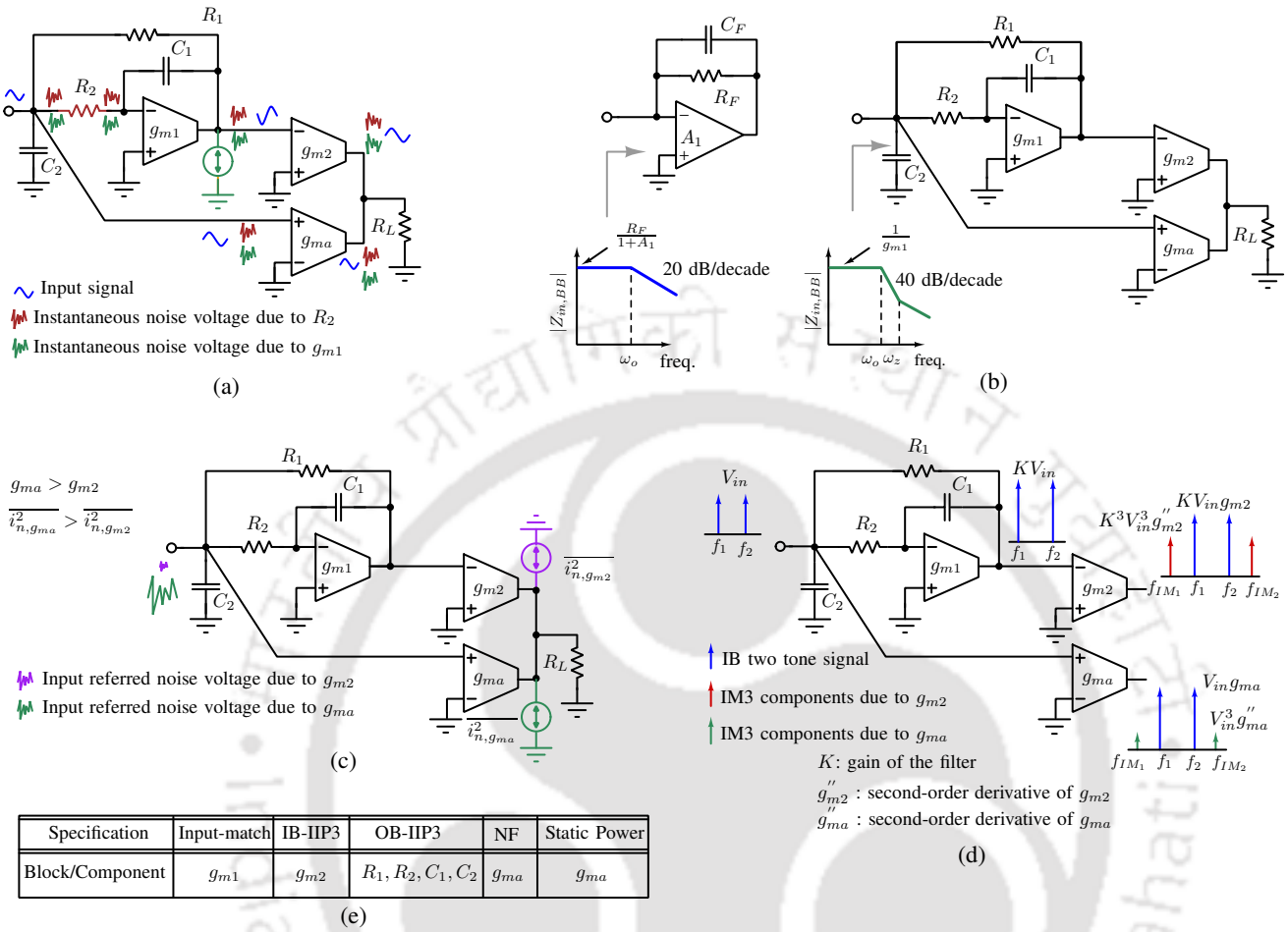
The proposed TIA uses transconductors rather than operational amplifier(s). In the following subsections, the advantages of using an operational transconductance amplifier (OTA) based TIA are briefly reviewed first. A description and the analysis of the proposed TIA are presented in Section 5.4-5.5.

5.3.1 OTA based TIA

A TIA can be designed using either an opamp or an OTA. The performance tradeoffs in both these implementations are studied in [78]. A brief summary of these tradeoffs is presented here. Whenever the TIA is designed to have an input impedance (R_{in}) of $\approx R_F/A_v$, where R_F is the feedback resistor of the TIA, the TIA exhibits low noise behavior but poor linearity. A TIA with $R_{in} \approx R_F/A_v$ is said to be operating in a linearity-limited regime [78]. In an opamp based TIA, A_v is the dc gain of the opamp. In an OTA based TIA, $A_v = G_m R_0$, where G_m is the transconductance and R_0 is the output impedance of the OTA. An OTA based TIA can also be designed to have an input impedance of $\approx 1/G_m$. In this scenario, the TIA exhibits good linearity characteristics but poor noise performance. A TIA with $R_{in} \approx 1/G_m$ is said to be operating in a noise-limited regime [78]. One can note that an opamp based TIA always operates in a linearity-limited regime. In the proposed architecture, an OTA based TIA is designed to operate in the noise-limited regime, and then the baseband noise cancellation scheme is used to improve the noise performance of the TIA.

5.3.2 Proposed second-order TIA

Fig. 5.6(a) shows the proposed baseband NC TIA. The main path of the proposed TIA consists of a Rauch filter using a matching transconductor g_{m1} and a second transconductance stage g_{m2}. The auxiliary path consists of a third baseband transconductor g_{ma} as shown in Fig. 5.6(a). The passive



Specification	Input-match	IB-IIP3	OB-IIP3	NF	Static Power
Block/Component	g_{m1}	g_{m2}	R_1, R_2, C_1, C_2	g_{ma}	g_{ma}

(e)

Figure 5.6: (a) Proposed baseband TIA using a second-order baseband NC scheme. Illustration of (b) input-match and OB-IIP3, (c) NF, and (d) IB-IIP3 using the proposed TIA. (e) Design blocks/components of the proposed mixer-first receiver.

components R_1, R_2, C_1, and C_2 contribute two poles and a zero to the input impedance of the TIA. Hence the TIA exhibits 40 dB/decade input impedance roll-off near the cut-off frequency, as shown in Fig. 5.6(b). After the zero frequency, the roll-off reduces to 20 dB/decade. A steeper impedance roll-off improves the OB-IIP3 of the receiver at close-in offset frequencies [65]. The impedance roll-off in a typical opamp based TIA is also shown in Fig. 5.6(b). In the proposed TIA, the instantaneous noise voltages due to g_{m1} at the input and output are in-phase. The noise voltage at the input is processed through the auxiliary transconductor g_{ma}, and the noise voltage at the output is processed through the second transconductor g_{m2}, as shown in Fig. 5.6(a). The output currents of g_{ma} and g_{m2} consists of a noise component due to g_{m1}. The noise components due to g_{m1} at the outputs of g_{ma} and g_{m2} are in out-of-phase with each other. When the output currents of g_{ma} and g_{m2} are combined,

the noise due to g_{m1} can be canceled without affecting the input signal. Similarly, the noise due to the resistor R_2 can also be canceled by combining the output currents of g_{ma} and g_{m2}. After the cancellation of g_{m1} noise, one has to consider the noise due to g_{m2} and g_{ma}. For noise cancellation, the gain of the main path and the auxiliary paths needs to be equal. This requires g_{ma} to be greater than g_{m2}. Since $g_{ma} > g_{m2}$, the noise contribution of g_{ma} is also greater than the noise contribution of g_{m2}, as shown in Fig. 5.6(c). Another way of understanding this noise behavior is that the noise contribution of the g_{m2} is suppressed by the gain of the Rauch filter. Therefore the NF of the TIA is dominated by the NF of the g_{ma}.

The noise cancellation technique also acts as a distortion cancellation technique and the distortion due to g_{m1} is also cancelled at the combined output of g_{m2} and g_{ma}. Between g_{m2} and g_{ma}, the distortion due to g_{m2} is greater than the distortion due to g_{ma}. Fig. 5.6(d) explains the distortion due to g_{m2} and g_{ma} with the help of two tones. If we apply two IB tones of equal magnitude (V_{in}) to the TIA, then g_{m2} sees an amplified version of the tones at its input. Let K be the gain of the Rauch filter and the filter is assumed to be ideal. Then the output current of g_{m2} consists of third-order inter-modulation products (IM3) of magnitude $g''_{m2}(K^3V^3_{in})$, where g''_{m2} is the second derivative of g_{m2}. The magnitude of IM3 components in g_{ma} would be $g''_{ma}(V^3_{in})$, where g''_{ma} is the second derivative of g_{ma}. For noise-and-distortion cancellation, we need $g_{ma} = Kg_{m2}$. If we assume K copies of g_{m2} blocks are used in parallel for the realization of g_{ma}, then $g''_{ma} \approx Kg''_{m2}$. Therefore the magnitude of IM3 components in the output current of g_{m2} is higher than the magnitude of IM3 components in the output current of g_{ma}. Hence, the linearity of the proposed TIA is limited by the linearity of the g_{m2} block.

A summary of the above discussion is shown in Fig. 5.6(e). The input impedance of the proposed TIA can be independently adjusted by adjusting the g_{m1} value alone. The NF of the proposed TIA (and hence the receiver) is dominated by the NF of the auxiliary transconductor g_{ma}. The linearity of the g_{m2} block limits the IB-IIP3 of the proposed TIA. The close-in OB-IIP3 can be slightly adjusted by adjusting the passive components of the Rauch filter. The auxiliary transconductor dominates the power consumption of the TIA, since $g_{ma} > g_{m2}$.

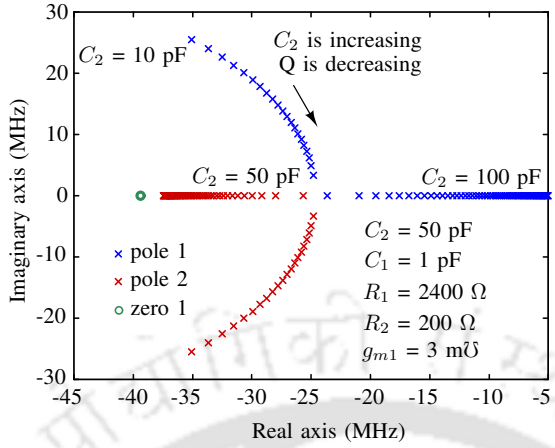


Figure 5.7: Pole-Zero diagram of the input impedance of the proposed TIA.

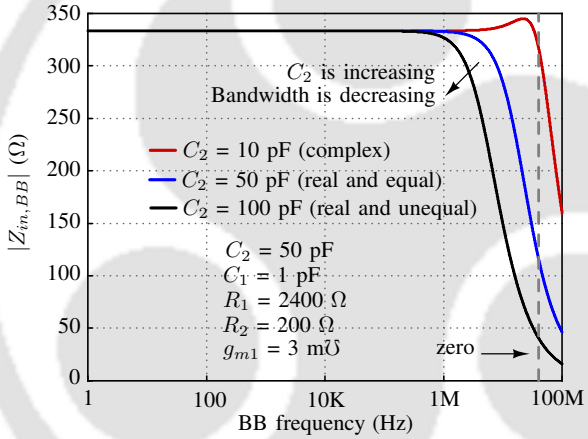


Figure 5.8: Magnitude of the input impedance of the proposed TIA for various poles.

5.3.3 Theoretical analysis

The input impedance of the proposed TIA is

$$Z_{in,BB}(s) = \frac{\omega_{o,zin}^2}{g_{m1}} \frac{(1+\frac{s}{\omega_z})}{s^2 + \frac{\omega_{o,zin}}{Q_{zin}}s + \omega_{o,zin}^2}, \tag{5.10}$$

$$\text{where } \omega_z = \frac{1}{(R_1 + R_2 + g_{m1}R_1R_2)C_1}, \tag{5.11}$$

$$\omega_{o,zin} = \sqrt{\frac{g_{m1}}{C_1C_2(g_{m1}R_1R_2 + R_1 + R_2)}}, \tag{5.12}$$

$$\text{and } Q_{zin} = \frac{1}{\omega_{o,zin}(R_1C_1 + R_2C_1 + \frac{C_2}{g_{m1}})}. \tag{5.13}$$

Equations (5.10)-(5.13) show that the proposed TIA is stable with two left-half poles and one left-half zero. Depending on the quality factor (Q_{zin}), the two poles can be real or complex conjugate. To

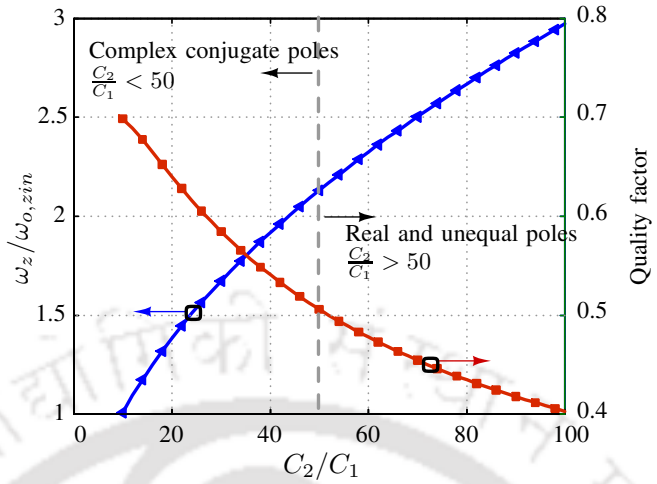


Figure 5.9: Ratio of $\omega_z/\omega_{o,zin}$ and Q_{zin} of the input impedance of the proposed TIA for various capacitance ratios C_2/C_1. In this simulation, 1 pF is used for C_1.

achieve a 40 dB/decade slope from the 3-dB frequency, one has to design the TIA to have either a pair of complex conjugate poles or two identical real poles. This requires Q_{zin} to be $\geq \frac{1}{2}$. The location of the zero depends on the capacitance C_1. Fig. 5.7 shows a simulated pole-zero diagram of the TIA input impedance. In this simulation, the following parameters are used: R_1=2.4 kΩ, R_2=200 Ω, C_1=1 pF and g_{m1}=3 mʊ. From Fig. 5.7, the complex conjugate poles move towards the real axis as the capacitance C_2 increases. Therefore, the Q_{zin} of the system decreases. Fig. 5.8 shows the simulated magnitude of the input impedance of the TIA for various poles. From Fig. 5.8, the bandwidth of the system decreases with an increase in the capacitance C_2. One has to keep the zero far away from the location of the poles to maintain the 40 dB/decade roll-off till the required frequency offset.

5.3.4 Limitation of the TIA under the input-matching constraint

In the proposed second-order TIA, it is not possible to achieve a high Q_{zin} for the filter while keeping the zero far-way from the location of poles. This limitation stems from the fact that g_{m1} is always set to a particular value to achieve the impedance matching. To keep the zero far-away from poles, we need to maximize the ratio $\omega_z/\omega_{o,zin}$. From (5.11)-(5.12),

$$\frac{\omega_z}{\omega_{o,zin}} = \sqrt{\frac{C_2}{C_1 g_{m1}(R_1 + R_2 + g_{m1}R_1R_2)}}. \tag{5.14}$$

From the above expression and under the matching constraint, the ratio $\omega_z/\omega_{o,zin}$ can be increased by increasing the ratio C_2/C_1. From (5.13), Q_{zin} of the filter decreases with an increase in C_2/C_1.

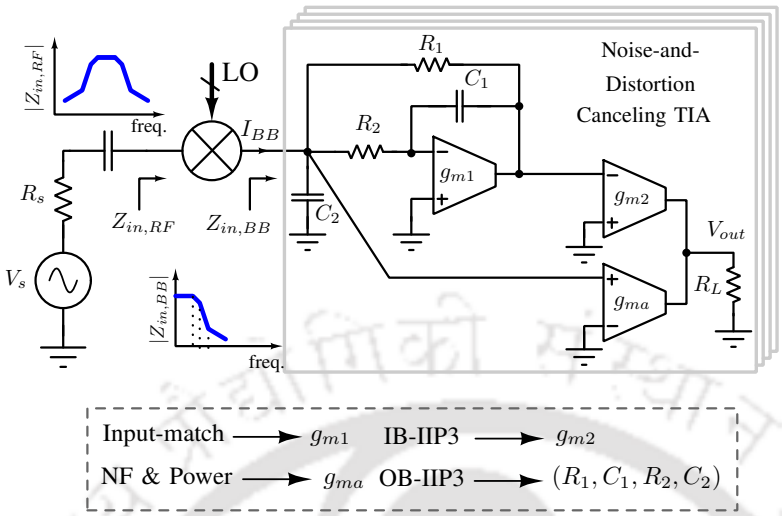


Figure 5.10: Proposed mixer-first receiver using the second-order baseband NC scheme.

Fig. 5.9 shows the variation of $\omega_z/\omega_{o,zin}$ and Q_{zin} with C_2/C_1. Fig. 5.9 clearly shows that it is not possible to simultaneously maximize both $\omega_z/\omega_{o,zin}$ and Q_{zin}. Design of the TIA with $Q_{zin} > 0.707$ gives complex poles but the the zero appears close to the cut-off frequency. An optimum choice is to design the TIA for equal and real poles which results in $Q_{zin} = 0.5$ and $\omega_z/\omega_{o,zin} \approx 2.2$.

Without-loss-of-generality, the impedance roll-off can be further improved by incorporating shunt-notch element as in [69], [85] at the TIA input. This can further enhance the OB-IIP3 of the receiver at close-in offset frequencies.

5.4 Receiver

Fig. 5.10 shows the proposed receiver architecture. In this section, we show through rigorous analysis that each performance metric of the receiver depends on the design of a specific sub-block of the TIA. The implementation details of these sub-blocks are discussed in the next section.

5.4.1 Input Impedance

An equivalent LTI model of the receiver [52] is shown in Fig. 5.11(a). In Fig. 5.11(a), R_s is the source resistance, R_{sw} is the on-resistance of the switch, R_{sh} accounts for the power lost due to up-conversion of the input signal, R_B represents the resistance looking into the TIA input, and γ represents a constant that depends on the number of paths. In Fig. 5.11(a), the impedance $Z_{in,BB}$ represents the baseband impedance and should be evaluated at the intermediate frequency $(\omega_{RF} - \omega_{LO})$. The

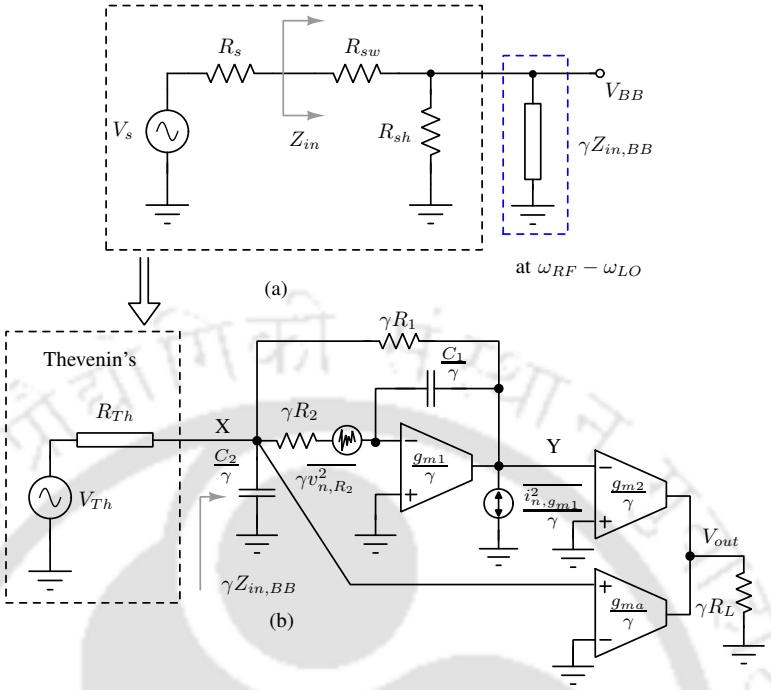


Figure 5.11: (a) Equivalent LTI model of an N-path mixer-first receiver. (b) Input impedance of the TIA per path.

input impedance Z_{in} of the receiver around the fundamental frequency is given by

$$Z_{in}(s) = R_{sw} + (R_{sh}||\gamma Z_{in,BB}(s)), \tag{5.15}$$

where

$$\gamma = \frac{sinc(\frac{\pi}{N})^2}{N}, \tag{5.16}$$

and

$$R_{sh} = (R_s + R_{sw})\frac{N\gamma}{1 - N\gamma}. \tag{5.17}$$

From (5.10), the dc input impedance of the TIA is equal to $1/g_{m1}$. In a four-path mixer-first receiver, we need $g_{m1} \approx 3$ m℧ to achieve 50 Ω input-match at the RF input. Fig. 5.12 shows a comparison of the simulated and analytical (5.15) input impedance of the receiver.

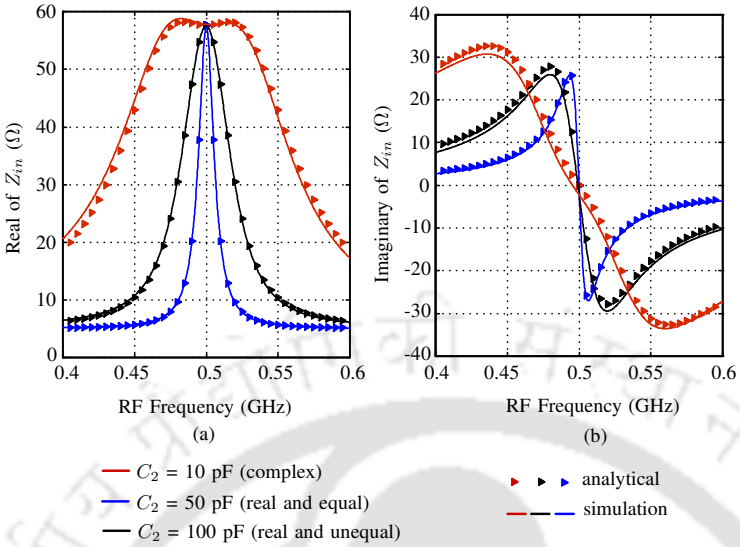


Figure 5.12: Input impedance of the proposed receiver for various poles.

5.4.2 Gain

To compute the conversion gain of the receiver, the LTI model can be replaced by an equivalent Thevenin model, as shown in Fig. 5.11(b). In Fig. 5.11(b), the baseband resistance $\gamma Z_{in,BB}$ is replaced by an equivalent single-ended NC TIA with appropriate scaling factors. The Thevenin voltage (V_{Th}) and the open-circuit impedance (R_{Th}) are

$$V_{Th} = \frac{R_{sh}}{R_a + R_{sh}} V_s, \tag{5.18}$$

$$R_{Th} = R_a || R_{sh}, \tag{5.19}$$

where $R_a = R_s + R_{sw}$. The voltages at nodes X, Y and output are given by

$$V_X(s) = \frac{K\big[1 + sC_1(R_1 + R_2 + R_1R_2g_{m1})\big]}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} V_{Th}, \tag{5.20}$$

$$V_Y(s) = \frac{K\big[1 - R_1g_{m1} + sC_1(R_1 + R_2)\big]}{s^2 + \frac{\omega_o}{Q}s + \omega_o^2} V_{Th}, \tag{5.21}$$

$$V_{out}(s) = \big[-g_{m2}V_Y(s) + g_{ma}V_X(s)\big]R_L V_{Th}, \tag{5.22}$$

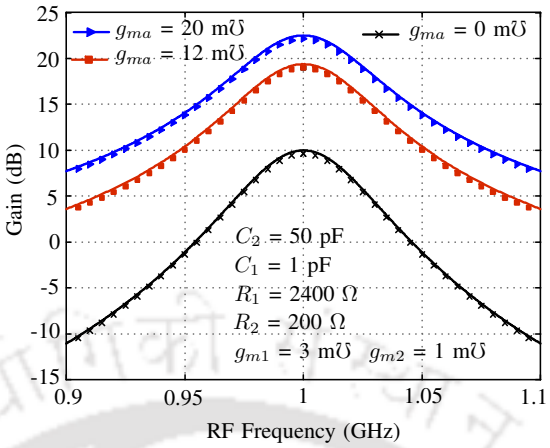


Figure 5.13: Gain of the receiver for various g_{ma} values. Marker indicates the analytical (5.23) results and solid line indicates the simulation results.

where

$$
\begin{aligned}
K &= \frac{\gamma\omega_o^2}{\gamma + g_{m1}R_{Th}},\\
\omega_o &= \sqrt{\frac{\gamma + g_{m1}R_{Th}}{C_1C_2R_{Th}(R_1 + R_2 + R_1R_2g_{m1})}},\\
Q &= \frac{\omega_o C_1C_2R_{Th}(R_1R_2g_{m1} + R_1 + R_2)}{\big[X + C_2R_{Th} + \gamma C_1(R_1 + R_2)\big]},\\
X &= C_1g_{m1}(R_1R_{Th} + R_2R_{Th} + \gamma R_1R_2).
\end{aligned}
$$

The voltage gain of the receiver is given by

$$G(s) = \frac{V_{out(s)}}{V_s(s)} = \frac{R_{sh}}{R_{sh} + R_a}\big[-g_{m2}V_Y(s) + g_{ma}V_X(s)\big]R_L. \tag{5.23}$$

Fig. 5.13 shows a comparison of the simulated and analytical (5.23) voltage gains of the receiver for different g_{ma} values at $f_{RF} = 1$ GHz. In this simulation the following parameters are used: $R_{sw} = 5\ \Omega$, $R_L = 1$ kΩ, $C_1 = 1$ pF, $C_2 = 50$ pF, $g_{m1} = 3$ m℧, $g_{m2} = 1$ m℧, $R_1 = 2.4$ kΩ and $R_2 = 200\ \Omega$.

From (5.20), (5.21) and (5.23) DC gain at various nodes is given by

$$G_X = \frac{V_X}{V_s} = \left[\frac{1}{1 + \frac{g_{m1}}{\gamma}R_{Th}}\right]\frac{R_{Th}}{R_a}, \tag{5.24}$$

$$G_Y = \frac{V_Y}{V_s} = \left[\frac{1 - g_{m1}R_1}{1 + \frac{g_{m1}}{\gamma}R_{Th}}\right]\frac{R_{Th}}{R_a}, \tag{5.25}$$

$$G_{out} = \frac{V_{out}}{V_s} = \left[\frac{-g_{m2}(1 - g_{m1}R_1) + g_{ma}}{1 + \frac{g_{m1}}{\gamma}R_{Th}}\right]\frac{R_{Th}R_L}{R_a}. \tag{5.26}$$

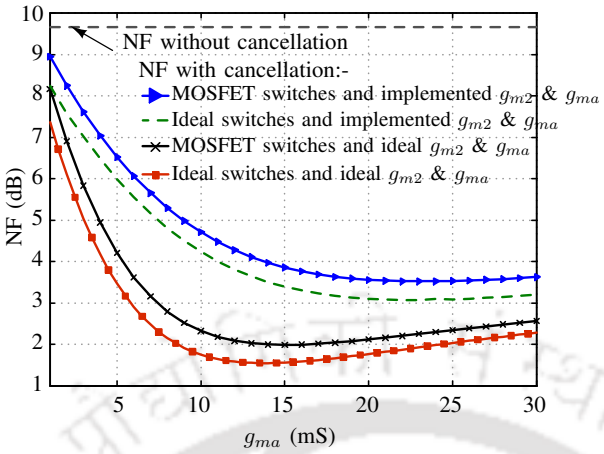


Figure 5.14: Simulated NF of the receiver for various g_{ma} values.

5.4.3 Noise

5.4.3.1 Noise-canceling condition

In the proposed second-order NC TIA, the noise of g_{m1} as well as the noise of R_2 can be canceled at the output. In Fig. 5.11(b), $\overline{i_{n,g_{m1}}}$ and $\overline{v_{n,R_2}}$ represent the noise current due to g_{m1} and the noise voltage due to R_2, respectively. The instantaneous noise voltages at nodes X and Y due to $\overline{i_{n,g_{m1}}}$ and $\overline{v_{n,R_2}}$ are

$$v_{n,X} = \frac{R_{Th}}{1+\frac{g_{m1}}{\gamma}R_{Th}}\left[\frac{\overline{i_{n,g_{m1}}}}{\sqrt{\gamma}} + \frac{\overline{v_{n,R_2}}g_{m1}}{\sqrt{\gamma}}\right], \tag{5.27}$$

$$v_{n,Y} = \frac{R_{Th}+\gamma R_1}{1+\frac{g_{m1}}{\gamma}R_{Th}}\left[\frac{\overline{i_{n,g_{m1}}}}{\sqrt{\gamma}} + \frac{\overline{v_{n,R_2}}g_{m1}}{\sqrt{\gamma}}\right]. \tag{5.28}$$

For noise cancellation at the output, the noise currents at the outputs of g_{m2} and g_{ma} should be equal in magnitude.

$$\begin{aligned} g_{m2}v_{n,Y} &= g_{ma}v_{n,X} \\ \frac{g_{ma}}{g_{m2}} &= 1+\frac{\gamma R_1}{R_{Th}} \end{aligned} \tag{5.29}$$

From (5.19), (5.29) can be written as

$$\frac{g_{ma}}{g_{m2}} = 1+\frac{\gamma R_1}{R_a||R_{sh}}. \tag{5.30}$$

From (5.23) and (5.30), the dc voltage gain under the NC condition is

$$G_{NC} = g_{m2}\frac{\gamma R_1 R_L}{R_a}. \tag{5.31}$$

The NC condition (5.30) is verified through simulations of the receiver with the ideal as well as implemented g_{m2} and g_{ma}. The implementation details of the Rauch filter, g_{m2} and g_{ma} are discussed in the next section. Fig. 5.14 shows the variation of NF of the receiver with g_{ma} at 1 MHz. In this simulation, $R_{sw} = 5\ \Omega$, $R_L = 1\ \text{k}\Omega$, $C_1 = 1$ pF, $C_2 = 50$ pF, $g_{m1} = 3$ m℧, $g_{m2} = 1$ m℧, $R_1 = 2.4\ \text{k}\Omega$ and $R_2 = 200\ \Omega$ are used.

5.4.3.2 Noise Factor

Let $\overline{v_{n,s}^2} = 4kTR_s$, $\overline{v_{n,sw}^2} = 4kTR_{sw}$, $\overline{v_{n,sh}^2} = 4kTR_{sh}$, $\overline{v_{n,R_1}^2} = 4kTR_1$ and $\overline{v_{n,R_2}^2} = 4kTR_2$ represent the mean square thermal noise voltage densities of the resistors R_s, R_{sw}, R_{sh}, R_1 and R_2 respectively. Let $\overline{i_{n,g_{m1}}^2}$, $\overline{i_{n,g_{m2}}^2}$ and $\overline{i_{n,g_{ma}}^2}$ represent the mean square thermal noise current densities at the outputs of g_{m1}, g_{m2} and g_{ma} respectively.

When noise cancellation is OFF (auxiliary path is disabled), the total noise voltage across γR_L is

$$\begin{aligned}\overline{v_{n,out}^2} = G^2\Big(\overline{v_{n,s}^2} + \overline{v_{n,sw}^2} + \left[\frac{R_a}{R_{sh}}\right]^2\overline{v_{n,sh}^2}\Big) + \gamma\overline{v_{n,R_1}^2}g_{m2}^2R_L^2 \\ + g_{m2}^2R_L^2R_{out}^2\left[\frac{\overline{i_{n,g_{m1}}^2}}{\gamma} + \frac{\overline{v_{n,R_2}^2}}{\gamma}g_{m1}^2\right] + \gamma\overline{i_{n,g_{m2}}^2}R_L^2,\end{aligned} \tag{5.32}$$

where

$$R_{out} = \frac{\gamma R_1 + R_{Th}}{1 + \frac{g_{m1}}{\gamma}R_{Th}}.$$

The total noise voltage at the output, under the noise cancellation (auxiliary path is enabled), is given by

$$\overline{v_{n,out}^2} = G_{NC}^2\Big(\overline{v_{n,s}^2} + \overline{v_{n,sw}^2} + \left[\frac{R_a}{R_{sh}}\right]^2\overline{v_{n,sh}^2}\Big) + \gamma\overline{v_{n,R_1}^2}g_{m2}^2R_L^2 + \gamma\overline{i_{n,g_{m2}}^2}R_L^2 + \gamma\overline{i_{n,g_{ma}}^2}R_L^2. \tag{5.33}$$

Using (5.33), the noise factor (F) can be computed as

$$F = 1 + \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left[\frac{R_a}{R_{sh}}\right]^2 + \frac{R_a^2}{\gamma R_1 R_s} + \frac{1}{G_{NC}^2 4kTR_s}\left(\gamma\overline{i_{n,g_{m2}}^2} + \gamma\overline{i_{n,g_{ma}}^2}\right)R_L^2. \tag{5.34}$$

From (5.30), one can recall that g_{ma} is larger than g_{m2} for noise cancellation. Therefore, the noise contribution of g_{ma} dominates the overall noise performance of the receiver. The noise factor can be

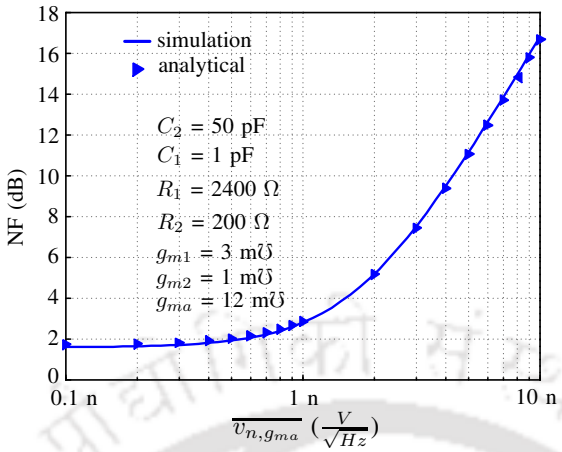


Figure 5.15: NF of the receiver for various noise voltages of g_{ma}.

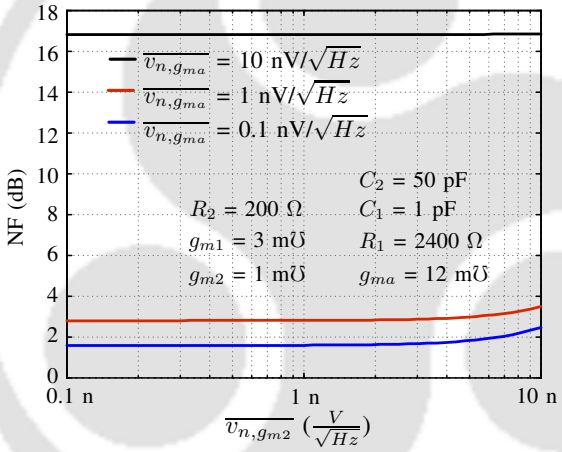


Figure 5.16: Simulated NF of the receiver for various noise voltages of g_{m2}.

approximated by

$$F = 1 + \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left[\frac{R_a}{R_{sh}}\right]^2 + \frac{R_a^2}{\gamma R_1 R_s} + \frac{1}{G_{NC}^2 4kTR_s}\gamma\overline{v_{n,g_{ma}}^2}g_{ma}^2R_L^2, \tag{5.35}$$

where

$$\overline{v_{n,g_{m2}}^2}g_{m2}^2 = \overline{i_{n,g_{m2}}^2} \quad \text{and} \quad \overline{v_{n,g_{ma}}^2}g_{ma}^2 = \overline{i_{n,g_{ma}}^2}. \tag{5.36}$$

The noise factor equation (5.35) is verified through simulations of the receiver for various input noise voltages ($\overline{v_{n,g_{ma}}}$) of g_{ma}. The tranconductor g_{m2} is assumed to be noiseless. In this simulation, the following parameters are used: R_{sw} = 5 Ω, R_L = 1 kΩ, C_1 = 1 pF, C_2 = 50 pF, g_{m1} = 3 m℧, g_{m2} = 1 m℧, g_{ma} = 12 m℧, R_1 = 2.4 kΩ and R_2 = 200 Ω. Fig. 5.15 shows the variation of NF of the

receiver with $\overline{v_{n,g_{ma}}}$ at 1 MHz. The equation (5.35) shows that NF of the receiver is decided by the input noise voltage of g_{ma}. To confirm the non-dependence of NF on g_{m2}, the receiver is simulated for different input noise voltages of g_{m2} while fixing $\overline{v_{n,g_{ma}}}$. Fig. 5.16 shows the variation of NF of the receiver with $\overline{v_{n,g_{m2}}}$ at 1 MHz. The simulated NF is constant and independent of $\overline{v_{n,g_{m2}}}$, as shown in Fig. 5.16.

Assuming $\overline{v_{n,g_{ma}}^2} = 4KT\gamma_M/g_{ma}$, the noise factor of the receiver can be further simplified by using (5.30), (5.31) and (5.35), and is given by

$$F = 1 + \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left[\frac{R_a}{R_{sh}}\right]^2 + \frac{R_a^2}{\gamma R_1 R_s} + \left[\frac{R_a}{R_1} + \frac{\gamma R_a}{R_{Th}}\right]^2 \frac{\gamma_M}{\gamma}\frac{1}{g_{ma}R_s} \tag{5.37}$$

From (5.37), the noise factor can be decreased by increasing the g_{ma}. Increasing g_{ma} requires large biasing current. The lower-bound on the noise factor ($\mathrm{F_{LB}}$) can be obtained from (5.37) when $g_{ma} \rightarrow \infty$. $\mathrm{F_{LB}}$ is given by

$$F_{LB} = 1 + \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left[\frac{R_a}{R_{sh}}\right]^2 + \frac{R_a^2}{\gamma R_1 R_s}. \tag{5.38}$$

Hence, the noise factor is ultimately limited by the mixer switch resistance.

5.4.4 Linearity

In general, the passive mixers are highly linear because of the good switching characteristics of transistors in scaled CMOS technologies. The NC technique also cancels the distortion due to the g_{m1} stage [45]. In the proposed receiver, the second transconductance stage g_{m2} and auxiliary path transconductance stage g_{ma} are the two sources of non-linearity. Let the output currents of g_{m2} and g_{ma} are

$$i_{out,g_{m2}} = (-g_{m2}V_Y - g_{m2}^{''}V_Y^3)/\gamma, \tag{5.39}$$

$$i_{out,g_{ma}} = (g_{ma}V_X + g_{ma}^{''}V_X^3)/\gamma, \tag{5.40}$$

where $g_{mi}^{''}$ represents the double-derivative of the g_{mi} with respect to the input voltage. The output voltage can be evaluated from (5.39) and (5.40) as

$$v_{out} = \big[-g_{m2}V_Y + g_{ma}V_X - g_{m2}^{''}V_Y^3 + g_{ma}^{''}V_X^3\big]R_L. \tag{5.41}$$

Using (5.29) in the above equation gives

$$v_{out} = \big[- g_{m2}V_Y + \big(1 + \frac{\gamma R_1}{R_{Th}}\big) g_{m2}V_X - g_{m2}^{''}V_Y^3 + g_{ma}^{''}V_X^3\big] R_L. \tag{5.42}$$

The term $g_{ma}^{''}V_X^3$ can be neglected, as $V_Y^3 \gg V_X^3$. Therefore, (5.42) is reduced to

$$v_{out} \approx \big[- g_{m2}V_Y + \big(1 + \frac{\gamma R_1}{R_{Th}}\big) g_{m2}V_X - g_{m2}^{''}V_Y^3\big] R_L. \tag{5.43}$$

Including non-linearity of switches into account, the thevenin voltage ${V_{Th}}^2$ is given by

$$V_{Th} = R_{sh}[\alpha_1 V_s + \alpha_3 V_s^3] \tag{5.44}$$

where α_1 and α_3 are linear and third-order conductance of MOSFET switches respectively. From (5.20), (5.21), (5.43) and (5.44), OB-IIP3 of the receiver is given by

$$\text{OB-IIP3} \approx \sqrt{\frac{4}{3}\left|\frac{1}{(\eta_{\text{sw}})^{-1} + (\eta_{\text{TIA}})^{-1}}\right|}, \tag{5.45}$$

where

$$\eta_{\text{sw}} = \frac{\alpha_1}{\alpha_3}$$

$$\eta_{\text{TIA}} = \frac{g_{m2}}{g_{m2}^{''}}\left[\frac{(1 + \frac{g_{m1}}{\gamma}R_{Th})^2 + \Delta\omega^2 C_1^2 R_X^2}{((1 - g_{m1}R_1)^2 + \Delta\omega^2 C_1^2 R_Y^2)^3}\right]^{\frac{1}{2}} \times \frac{\gamma R_1}{R_{Th}}\left[\left(1 - \frac{\Delta\omega^2}{\omega_o^2}\right)^2 + \frac{\Delta\omega^2}{\omega_o^2 Q^2}\right]\left(1 + \frac{g_{m1}}{\gamma}R_{Th}\right)^2 . \left(\frac{R_a}{R_{Th}}\right)^2$$

where $\Delta\omega$ is the offset from the center frequency, $R_X = R_1 + R_2 + R_1R_2g_{m1} + g_{m1}R_2\frac{R_{Th}}{\gamma}$ and $R_Y = R_1 + R_2$. As switches are more linear than TIA, the non-linearity due to switches can be ignored $(\eta_{\text{sw}} \gg \eta_{\text{TIA}})$[3] The OB-IIP3 is given by

$$\text{OB-IIP3} \approx \sqrt{\frac{4}{3}\left|\frac{g_{m2}}{g_{m2}^{''}}\left[\frac{(1 + \frac{g_{m1}}{\gamma}R_{Th})^2 + \Delta\omega^2 C_1^2 R_X^2}{((1 - g_{m1}R_1)^2 + \Delta\omega^2 C_1^2 R_Y^2)^3}\right]^{\frac{1}{2}}\right| \times}$$
$$\sqrt{\frac{\gamma R_1}{R_{Th}}\left[\left(1 - \frac{\Delta\omega^2}{\omega_o^2}\right)^2 + \frac{\Delta\omega^2}{\omega_o^2 Q^2}\right]}\left(1 + \frac{g_{m1}}{\gamma}R_{Th}\right) . \frac{R_a}{R_{Th}}, \tag{5.46}$$

[2] V_{Th} can be derived in the similar way as given in the Appendix B

[3] The IB-IIP3 and OB-IIP3 of the receiver (including only switches non-linearity) is computed in the Appendix B using MOSFET square-law model. Fig.B.3 of the Appendix B shows that typical IIP3 value of the MOSFET switches is more than +20 dBm for a on-resistance of 25 Ω. Hence, the contribution of switches non-linearity can be neglected.

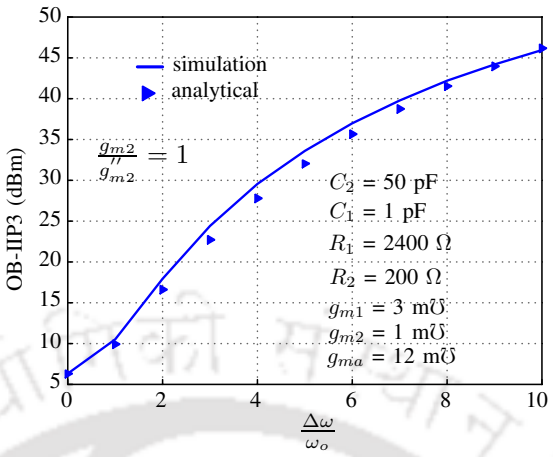


Figure 5.17: OB-IIP3 of the receiver for various $\Delta\omega/\omega_o$.

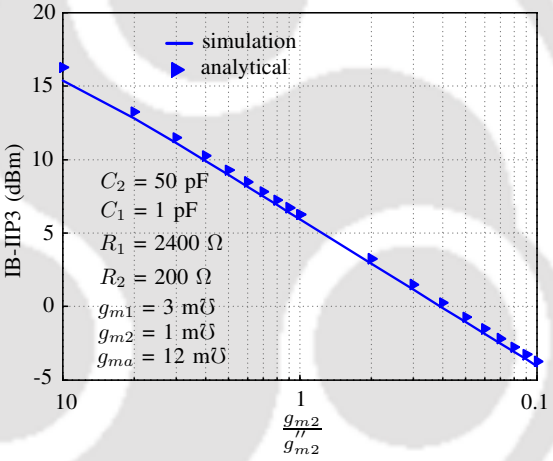


Figure 5.18: IB-IIP3 of the receiver for various g_{m2}/g''_{m2}.

In the passband where $\Delta\omega \to 0$, the OB-IIP3 converges to IB-IIP3. Hence, IB-IIP3 can be computed from (5.46) and is given by

$$\text{IB} - \text{IIP3} \approx \sqrt{\frac{4}{3}\left|\frac{g_{m2}}{g''_{m2}}\frac{\gamma R_1(1+\frac{g_{m1}}{\gamma}R_{Th})^3}{R_{Th}(1-g_{m1}R_1)^3}\right|}\frac{R_a}{R_{Th}}. \tag{5.47}$$

The OB-IIP3 equation (5.45) and IB-IIP3 equation (5.47) are verified through simulations of a mixer-first receiver using a non-linear model of g_{m2}. The tranconductor g_{ma} is considered to be linear with $g''_{ma} = 0$. In this simulation, the following parameters are used: $R_{sw} = 5\ \Omega$, $R_L = 1$ kΩ, $C_1 = 1$ pF, $C_2 = 50$ pF, $g_{m1} = 3$ m℧, $g_{m2} = 1$ m℧, $g_{ma} = 12$ m℧, $R_1 = 2.4$ kΩ and $R_2 = 200\ \Omega$. Fig. 5.17 shows the variation of OB-IIP3 with $\Delta\omega/\omega_o$. Fig. 5.18 shows the variation of IB-IIP3 with g_{m2}/g''_{m2}.

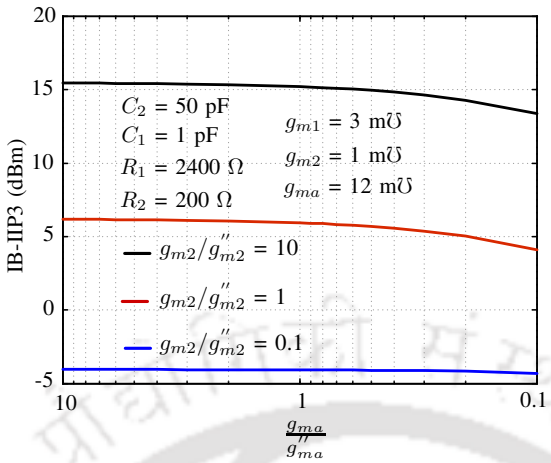


Figure 5.19: Simulated IB-IIP3 of the receiver for various g_{ma}/g''_{ma}.

One can infer from (5.47), that the IB-IIP3 of the complete receiver is limited by the IB-IIP3 of the second transconductance stage g_{m2}. To confirm the non-dependence of the IB-IIP3 on g_{ma}, the receiver is simulated with the non-linear model of g_{ma} as well. Fig. 5.19 shows the variation of IB-IIP3 with g_{ma}/g''_{ma} for different g_{m2}/g''_{m2} values. The simulated IB-IIP3 is constant and independent of g_{ma}/g''_{ma}, as shown in Fig. 5.19. When $\Delta\omega \to \infty$, ${\eta_{\text{TIA}}}^{-1} \to 0$. Therefore, saturated OB-IIP3 depends on the mixer switches [79] and is given by given by

$$\text{OB} - \text{IIP3}_{\text{sat.}} \approx \sqrt{\frac{4}{3}|\eta_{\text{sw}}|} \approx \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{5.48}$$

5.4.5 Static Power

The static power consumption of the receiver is only due to the NC TIA. Assuming that each transconductor is designed to operate with a $g_m/I_D = r$, we can estimate the typical power consumption of each block. Let I_1, I_2 and I_a are bias currents of the three transconductors g_{m1}, g_{m2}, and g_{ma}, respectively. For input-matching, we need $g_{m1} = 3$ m℧. Therefore, $I_1 = \frac{3}{r}$ mA. Noise cancellation occurs when $g_{ma} = (1 + \frac{\gamma R_1}{R_{Th}})g_{m2}$. Therefore, $I_a = (1 + \frac{\gamma R_1}{R_{Th}})I_2$. In the actual implementation, we have chosen $g_{m2} = 1$ m℧, $R_1 = 2.4$ $k\Omega$. This results in the bias currents of $I_2 = \frac{1}{r}$ mA and $I_a = \frac{12}{r}$ mA. The total current requirement of the TIA is $\frac{16}{r}$ mA, out of which g_{ma} consumes $\frac{12}{r}$ mA of current. Therefore the static power consumption is dominated by the g_{ma} stage. Any linearization technique to improve the linearity of g_{m2} may increase the power consumption further.

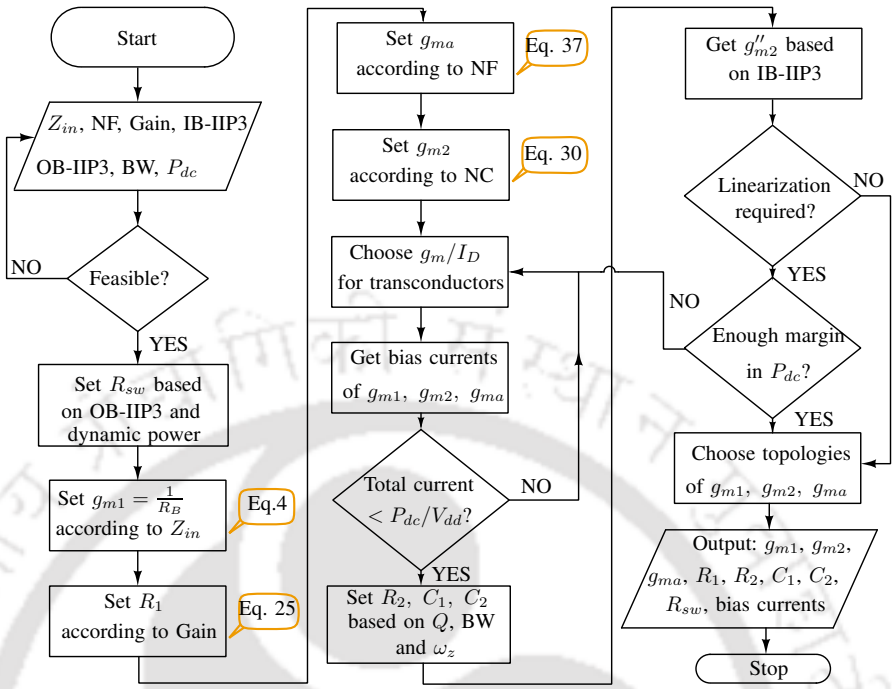


Figure 5.20: Typical design flow of the proposed receiver.

5.5 Design Procedure and CMOS Implementation

The following input specifications are considered in this design flow: Z_{in} (or R_s), NF, IB-IIP3, OB-IIP3, gain, bandwidth (BW), number of paths (N), and power consumption (P_{dc}). Fig. 5.20 shows a flow-chart of the typical design procedure. The first step of the design procedure is to check the design feasibility. Probable checks include very small P_{dc}, very small NF, very high IIP3, very high Gain-BW product, etc. The size of the mixer switch should be chosen based on the OB-IIP3 requirement and the dynamic power consumption specification. The transconductance of the Rauch filter (g_{m1}) should be chosen based on the input-match requirement. One can estimate the g_{ma} required to achieve the desired NF using (5.37). Using the noise-canceling condition (5.30) and the g_{ma} value, one can estimate the required g_{m2} value. The bias currents of all the three transconductors can be obtained based on the chosen g_m/I_D values. We need to check the total power consumption and adjust the bias currents according to the given specification (P_{dc}). The values of remaining passive components R_2, C_1 and C_2 can be obtained based on the BW specification and (5.11)-(5.13). One can roughly calculate the g''_{m2} required to achieve the required IB-IIP3 and decide weather a linearization technique is necessary or not for g_{m2}. The complete block diagram of the implemented chip is shown in Fig. 5.21. The design

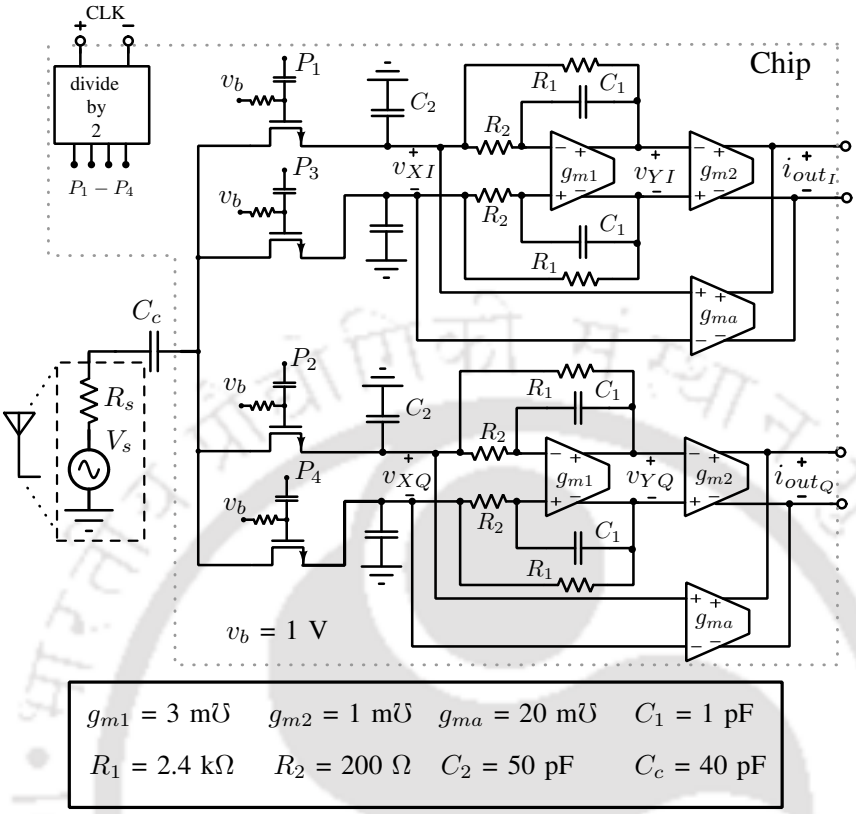


Figure 5.21: Complete block diagram of the implemented mixer-first receiver.

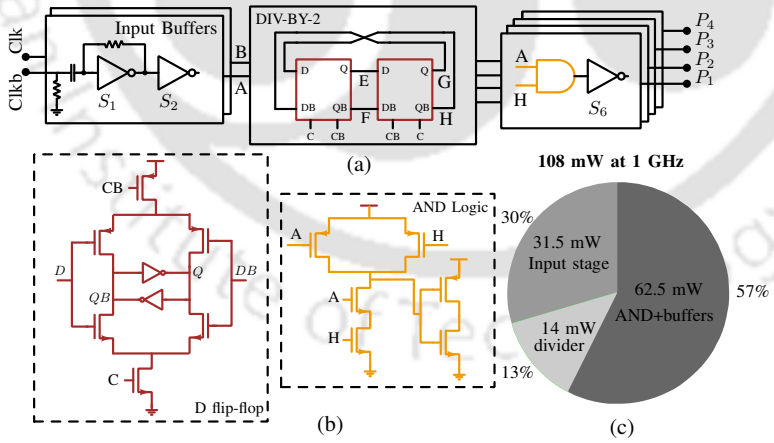


Figure 5.22: (a) Block diagram and (b) implementation of 4-phase clock generation. (c) Dynamic power consumption of the receiver at 1 GHz.

and implementation details of each block are given below.

5.5.1 Four-phase clock generation

The mixer switches are driven by 4-phase non-overlapping 25% duty-cycle clocks. The clock signals are generated using an on-chip frequency divider and a set of combinational digital circuits. Fig. 5.22(a) shows the block diagram the 4-phase clock generator. An off-chip differential clock signal at 2×LO frequency is used as an input to the clock generator. Fig. 5.22(b) shows the circuit diagrams of the D-latch and AND gate. The clock generation circuitry consumes 108 mW of power at 1 GHz. Fig. 5.22(c) shows the distribution of the dynamic power consumption of the receiver. The output buffers consume a major portion (57%) of the of the total dynamic power as they drive mixer switches with large width. The input buffers, which provide the broadband impedance matching, consume 31.5 mW of power at 2 GHz (i.e., 1 GHz LO frequency).

5.5.2 Mixer switches

In the current four-phase mixer implementation, NMOS transistors are used as switches. The mixer switches are dc coupled to the baseband TIA. This dc coupling forces the potential at source and drain terminals of switches to be $\approx V_{dd}/2$. This dc voltage reduces the overdrive voltage (V_{OD}) of switches which results in poor OB-IIP3. Using the square law model of the MOSFET, the OB-IIP3 of the mixer-first receiver can be shown to be as follows [86][4]

$$\text{OB} - \text{IIP3} = \sqrt{\frac{8}{3}\frac{(1+\rho)^4}{\rho^3}V_{OD}^2}, \tag{5.49}$$

where $\rho = R_{sw}/R_s$, R_{sw} is the switch resistance, and $V_{OD} = V_{GS} - V_{th}$ is the overdrive voltage of the switch. To improve the OB-IIP3, the mixer switches are biased using capacitive coupling at their gates. In the current implementation, V_{OD} is equal to $\approx$ 1.2 V. From (5.49), one has to choose small R_{sw} for a large OB-IIP3. A smaller R_{sw} requires a larger width for switches which results in a greater dynamic power consumption. In the current implementation, the switches are sized to have an ON resistance of 5 Ω. The corresponding NMOS transistor dimension is 150 μm/180 nm. Using (5.49), the estimated OB-IIP3 of the receiver is +47 dBm. Fig. 2 of Appendix B shows the theoretical OB-IIP3 of the receiver for various switch resistances.

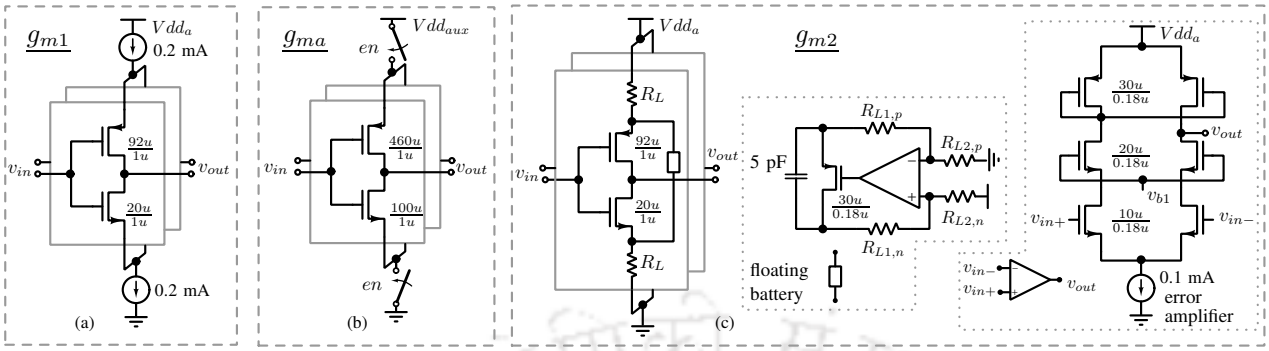


Figure 5.23: Circuit implementations of g_{m1}, g_{ma} and g_{m2}.

5.5.3 Baseband TIA

The baseband TIA is designed to have a bandwidth of $\approx$ 20 MHz. The zero in the TIA input impedance is at $\approx$ 40 MHz. Fig. 5.23 shows the schematic diagrams of the three transconductors g_{m1}, g_{ma}, and g_{m2}. CMOS inverter-based transconductor topologies are used for better linearity and NF. The component values and transistor sizing used in the current implementation are shown in Fig. 5.23.

From the input matching requirement, we need a $g_{m1} = 3$ m$\mho$. The noise and distortion due to g_{m1} are canceled by the NC scheme. Therefore, the g_{m1} can be optimized for smallest power consumption. A current biased differential inverter based transconductor topology, shown in Fig. 5.23(a), is chosen for g_{m1}. The transistors are sized to have an output common mode voltage of $V_{DD}/2$. The transistors are operating at a g_m/I_D of 15.

The auxiliary transconductor g_{ma} limits the overall noise performance of the receiver. We wanted to test the receiver without the auxiliary path also. Accordingly, enable switches are added in the supply and ground paths of the transconductor. The circuit level implementation of g_{ma} is shown in Fig. 5.23(b). The required g_{ma} value is 20 m$\mho$. Each inverter consumes 1.8 mA of current resulting in a g_m/I_D of $\approx$ 5.55 for each transistor.

The implementation of the second transconductor g_{m2} is critical for the receiver linearity. [87] discusses various techniques to improve the linearity of a transconductor. In this work, inverters with resistive source degeneration in both NMOS and PMOS are used for the implementation of g_{m2}. Further, a floating battery-based linearization technique [88] is used to improve the linearity of g_{m2}. The source voltages of PMOS and NMOS transistors of the degenerated inverter have fundamental

[4]The OB-IIP3 of the receiver (considering non-linearity of the switches) is also discussed in Appendix B.

component and second-order distortion. Due to the square law nature of the MOSFET, the second order distortion term mixes with the gate voltage and results in the third-order distortion components. At source nodes of PMOS and NMOS transistors, the fundamental components are in the same phase and second-order components are out-of-phase. The floating battery bypasses all the second-order components and improves the linearity of the transconductor. Each resistive degenerated transconductor is biased at a current of 0.3 mA with a g_m/I_D of 3.3. The current consumption of the total g_{m2} stage including the floating battery is 0.85 mA.

5.6 Measurement Results

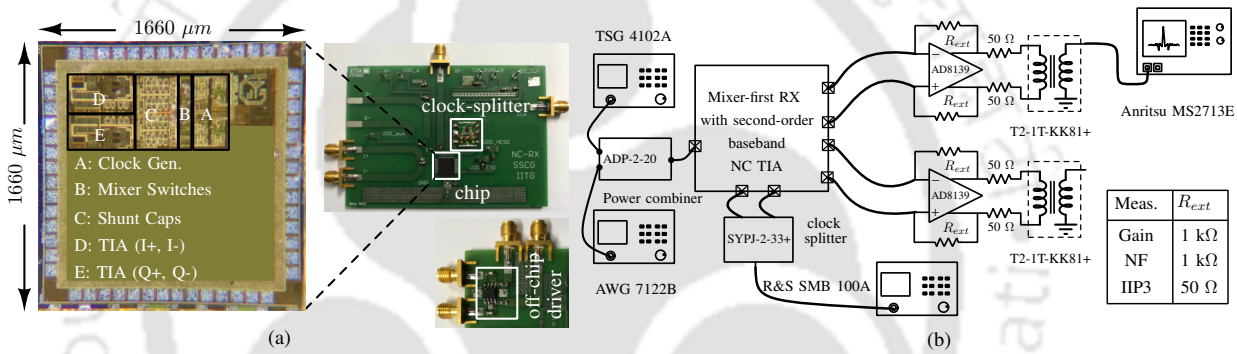


Figure 5.24: (a) Die micrograph and photographs of testing boards. (b) IIP3 measurement setup.

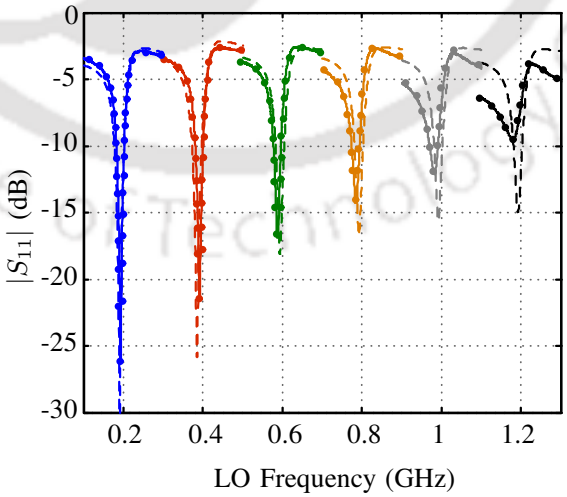


Figure 5.25: Measured $|S_{11}|$ of the receiver for different LO frequencies. Solid lines indicate measured results and dashed lines indicate the simulated results.

A prototype receiver is fabricated in CMOS 180 nm technology. The chip is enclosed in a 56-pin

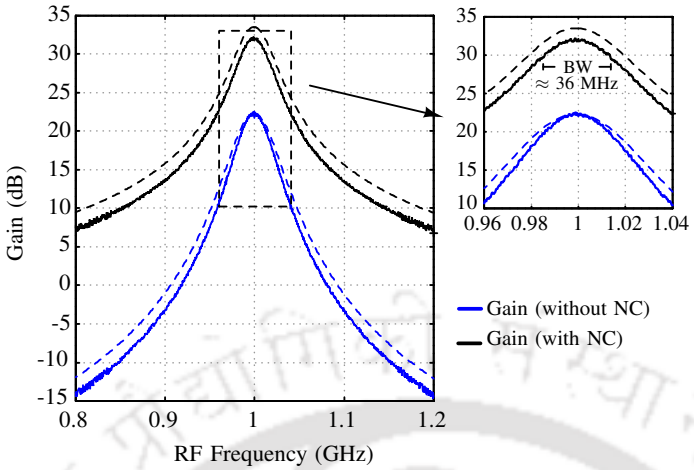


Figure 5.26: Measured voltage gain of the receiver at 1 GHz. Solid lines indicate measured results and dashed lines indicate the simulated results.

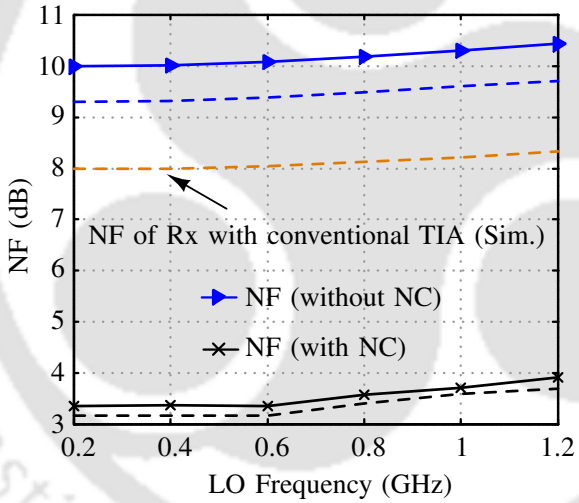


Figure 5.27: Measured NF of the receiver with and without NC. Solid lines indicate measured results and dashed lines indicate the simulated results.

QFN package and mounted on a printed circuit board (PCB) for testing. The photographs of the chip and testing boards are shown in Fig. 5.24(a). Fig. 5.24(a) also shows an off-chip driver board based on AD8139 opamp which is used to convert the output current to voltage. The driver is working on a 5 V supply and has high linearity. Fig. 5.24(b) shows the measurement setup of the receiver. For IIP3 measurements, a reduced feedback resistance R_{ext} of the driver is used so that IIP3 of the driver does not limit the large OB-IIP3 of the receiver.

The center frequency of the receiver is tunable from 0.2 to 1.2 GHz. Fig. 5.25 shows the measured

Table 5.1: Comparison with other mixer-first receivers

	This work		RFIC19 [85]	JSSC19 [72]	JSSC19 [73]	JSSC18 [65]	RFIC18 [69]	ISSCC17 [89]
Architecture	Mixer-first RX with 2^{nd} order BB NC TIA		Mixer-first RX with BB NC TIA	Mixer-first RX with 40 dB/dec roll-off	Mixer-first RX with bottom plate mixing	Mixer-first RX with capacitive +ve feedback	Mixer-first RX with shunting notch	FA with time interleaving
	without NC	with NC						
Technology	180 nm		22 nm	28 nm	28 nm	45 nm SOI	130 nm SiGe	65 nm
BB order	2		1	2	1	2	2	NA
Frequency range (GHz)	0.2-1.2		1-6	0.2-2	0.1-2	0.2-8	2-11	0.1-1
Gain (dB)	22.2	31.4	22	13	16	21	10-24	23
BB bandwidth	22	18	175	9	6.5	10	40	5
NF (dB)	10-10.4	3.4-4	2.5-5	4.3-7.6	4.1-10.3	2.3-5.4	11±1	7
IB-IIP3 (dBm)	4.6	14.5	9	5⋆	5⋆	0⋆	-2⋆	8
OB-IIP3 (dBm)	15.1 Δf/BW=2.2	25 Δf/BW=2.2	18 Δf/BW=5.7	33.3 Δf/BW=8.8	44 Δf/BW=12.3	39 Δf/BW=8	20 Δf/BW=1.75	21 Δf/BW=2.4
OB-IIP3$^{\dagger}_{\text{sat.}}$ (dBm)	36.4	39.8	NA	33.3	44	39	20	23
AC-IIP3‡ (dBm)	14.7	24.8	14⋆	15⋆	23⋆	16⋆	14⋆	20⋆
B1dB (dBm)	-4.1 Δf/BW=2.2	2.4 Δf/BW=2.2	NA	12 Δf/BW=6.6	13 Δf/BW=12.3	12 Δf/BW=8	1.8 Δf/BW=1.75	5 Δf/BW=2.4
IB-SFDR$^{\nabla}$ (dB)	72.2	83.2	80.3	76.4	76.6	74.4	67.3	76.6
OB-SFDR$^{\top}$ (dB)	79.2 Δf/BW=2.2	90.1 Δf/BW=2.2	86 Δf/BW=5.7	95 Δf/BW=8.8	101 Δf/BW=12.3	100 Δf/BW=8	82 Δf/BW=1.75	85 Δf/BW=2.4
Supply voltage (V)	1.8		0.83	1.2	1.2/1	1.2/1	4.5/2.5	1.2/1
Power (mW) Clock	45-135	45-135	172■	3.6-36	33◇	30◇	1466-1494	2-22
Power (mW) RX	6.8	19.8	NA	143	30	50	656	62
IBFOM (dBMHz/mW)	1.04	**13.52**	NA	-11.85	-5.26	-0.72	-22.22	-7.25
OBFOM (dB/mW)	-8.46	6.25	NA	1.71	4.27	**10.99**	-27.72	-2.24
ACFOM (dB/mW)	-19.33	**-1.97**	-7.45	-16.91	-9.02	-4.76	-33.5	-9.56
Area (mm^2)	0.54		0.48	0.48	0.49	0.8	5	2.3

⋆ estimated from figures; ◇ at 1 GHz; ∇ IB-SFDR=2/3(IB-IIP3+174-10log(1MHz)-NF); ⊤ OB-SFDR=2/3(OB-IIP3+174-10log(1MHz)-NF); ■ includes RX power; † OB-IIP3$_{\text{sat.}}$ = saturated OB-IIP3; ‡AC-IIP3 = Adjacent channel IIP3 which is OB-IIP3@ Δf/BW=2.

input return loss ($|S_{11}|$) of the receiver for different local oscillator (LO) frequencies. The receiver has $|S_{11}|$ less than -10 dB from 0.2-to-1.2 GHz. The gain and NF measurements are carried out with and without noise cancellation. Fig. 5.26 shows the measured voltage gain of the receiver at 1 GHz. The receiver has 31 dB gain and 36 MHz of RF bandwidth when noise cancellation is enabled. One can observe that the roll-off rate far-away from the 3-dB frequency is reduced when noise cancellation is enabled. This is due to the additional zero introduced by the g_{ma} stage in the voltage transfer function. Fig. 5.27 shows the NF of the receiver. The receiver has NF of ≈ 10 dB without noise cancellation, and this value comes down to 3-4 dB when noise cancellation is enabled.

The IB-IIP3 and OB-IIP3 measurements are also carried out with and without noise cancellation. Fig. 5.28 shows IB-IIP3 and OB-IIP3 of the receiver at different LO frequencies. The two input tones

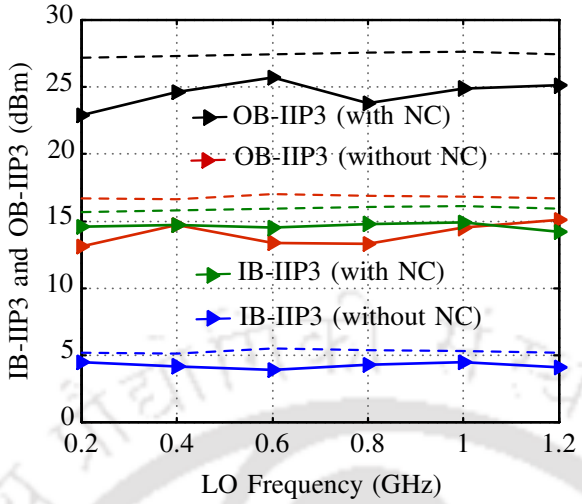


Figure 5.28: Measured IB-IIP3 and OB-IIP3 of the receiver at different LO frequencies. OB-IIP3 values are at $\frac{\Delta f}{\mathrm{BW}}$=2.2. Solid lines indicate measured results and dashed lines indicate the simulated results.

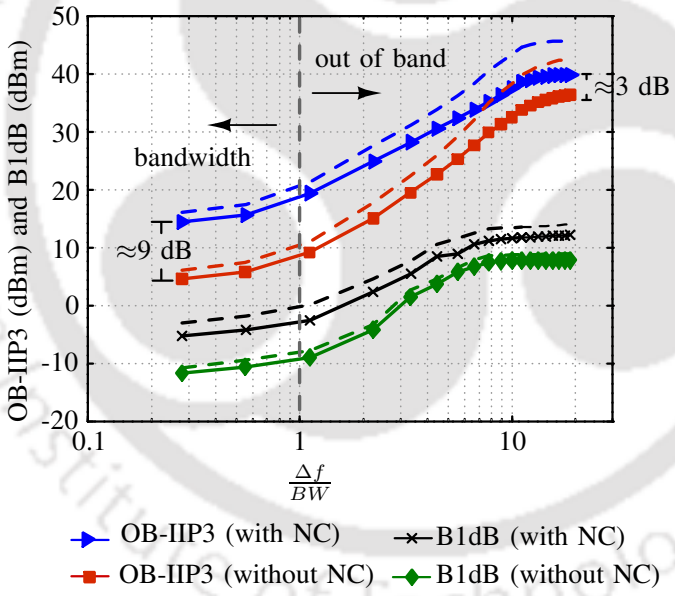


Figure 5.29: Measured OB-IIP3 and B1dB of the receiver for different frequency offset ($\frac{\Delta f}{\mathrm{BW}}$) at 1 GHz. Solid lines indicate measured results and dashed lines indicate the simulated results.

for OB-IIP3 measurements are at $f_1 = f_{LO} - \Delta f$ and $f_2 = f_{LO} - 2\Delta f + 1$ MHz, where f_{LO} is the LO frequency and Δf is the frequency offset. Without noise cancellation, the receiver has an average IB-IIP3 of 5 dBm and OB-IIP3 of 14 dBm at 40 MHz frequency offset. Without the auxiliary path, the linearity of the receiver is limited by the g_{m1} stage. After the cancellation of distortion due to g_{m1}, IIP3 of the receiver is limited by the g_{m2} stage as explained in Section II. The bottleneck of the

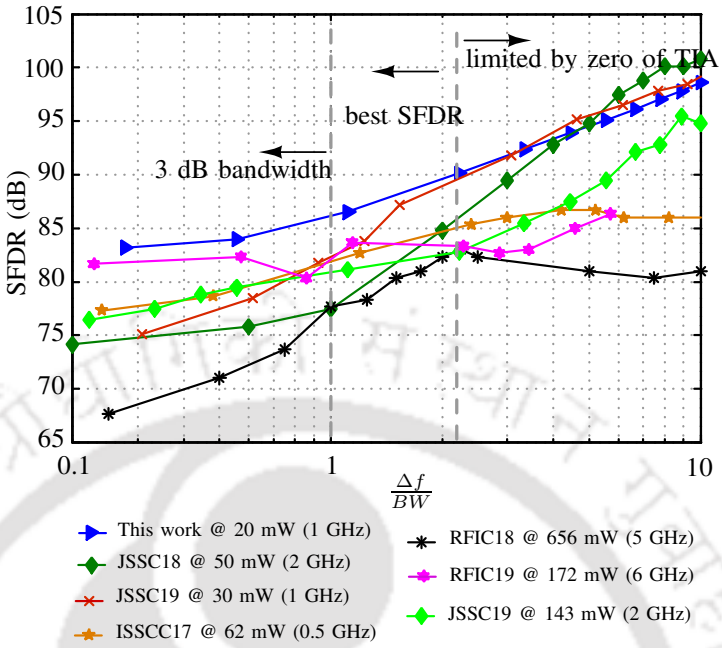


Figure 5.30: SFDRs of state-of-the-art mixer-first receivers with respect to the frequency offset.

Block	g_{m1}	g_{m2}	g_{ma}
Power (mW)	0.7	6.1	13
Power (%)	3	31	66

Figure 5.31: Static power consumption of the receiver.

linearity has moved from g_{m1} to g_{m2}. From Fig. 5.28, there is an improvement of greater than +9 dB in IB-IIP3 and OB-IIP3 values. Fig. 5.29 shows the measured OB-IIP3 and B1dB values at different frequency offsets from the 1 GHz LO frequency. At $\Delta f = 2.2 \times$ BW, the receiver has an IIP3 of +25 dBm and B1dB of +2.4 dBm.

Fig. 5.30 shows the spurious-free dynamic range (SFDR) of the receiver over the frequency offset and compares it with state-of-the-art mixer-first receivers. SFDR is calculated in 1 MHz bandwidth for all receivers. The proposed receiver has the highest SFDR for $\frac{\Delta f}{\text{BW}} < 3$ and lowest static power consumption. The clock path consumes 45-135 mW of power depending on the frequency of operation. The power consumption of the analog path is 19.8 mW. The g_{ma} stage limits the overall noise performance of the receiver and consumes $\approx 66\%$ of the TIA power. Fig. 5.31 shows the breakdown of the static power consumption of the receiver. Tab. I shows a full comparison of the current work with other mixer-first receivers.

The frequency of operation of the current receiver is limited by the clock divider circuit. A scaled CMOS technology can improve the frequency range. Moreover, a scaled CMOS technology also helps in reducing the dynamic (clock) power consumption. The receivers in [71] and [65] have lower NF than the current receiver. The receiver presented in this work has the highest IB-SFDR followed by the receiver in [85], which also uses the baseband NC scheme. The current receiver also has the highest OB-SFDR among all other receivers for a frequency offset less than 3×BW. The receivers in [65, 73] have ≥ 100 dB OB-SFDR for frequency offsets ≥ 8×BW.

5.6.1 Figure-of-Merits (FOMs)

For a fair comparison of this work with other mixer-first receivers, we have used three FOMs - one for the IB performance and the other two for the OB performance. The IBFOM is

$$\text{IBFOM} = 10\log_{10}\left(\frac{\text{G}\times\text{BW[MHz]}\times\text{IB\_IIP3[V]}}{\text{P}_\text{s}\text{[mW]}\times(\text{F}-1)\times\text{V}_\text{dd}\text{[V]}}\right), \tag{5.50}$$

where IB_IIP3 is the IB-IIP3 value expressed as an equivalent peak voltage across a 50 Ω resistor in volts, V_{dd} is the baseband supply voltage in volts, BW is the baseband bandwidth in MHz, G is the gain of the receiver and P_s is the static power consumption of the receiver (or TIA only) in mW. The IB performance of a mixer-first receiver mainly depends on the TIA performance and hence only the TIA power consumption is included in the IBFOM. The IIP3 value is normalized to the supply voltage to remove the undue advantage one may get by using a higher supply voltage (V_{dd}=1.8 V in this design).

In the case of OB performance, the size (and hence the resistance) of mixer switches determine the dynamic power consumption and the OB-IIP3 at far-away offset frequencies. Hence the FOM is modified to include the OB-IIP3 at far-away offset frequencies and the dynamic power consumption. The FOM used for OB performance is given below.

$$\text{OBFOM} = 10\log_{10}\left(\frac{\text{G}\times\text{OB\_IIP3}_{\text{sat.}}\text{[V]}}{\text{P}_\text{d}\text{[mW]}\times(\text{F}-1)\times\text{V}_\text{dd}\text{[V]}}\right), \tag{5.51}$$

where P_d is the dynamic power consumption at an LO frequency of 1 GHz. $\text{OB\_IIP3}_{\text{sat.}}$ is the saturated OB-IIP3 measured at far-away offset frequency. The $\text{OB\_IIP3}_{\text{sat.}}$ depends only on the linearity of mixer switches.

In the case of close-in offset frequencies, both the mixer switches and the TIA affect the receiver performance. Hence the FOM should include close-in OB-IIP3 and the total power consumption. In

a typical Frequency Division Duplexing (FDD) system, the nearest blocker can be in the adjacent channel (Δf/BW=2). Therefore, the following ACFOM is being proposed to compare the adjacent channel performance of receivers.

$$\text{ACFOM} = 10\log_{10}\left(\frac{\text{G} \times \text{AC\_IIP3[V]}}{\text{P}_\text{t}[\text{mW}] \times (\text{F}-1) \times \text{V}_\text{dd}[\text{V}]}\right), \tag{5.52}$$

where AC_IIP3 is the OB-IIP3 measured at an offset of Δf/BW=2, and P_t is the total power consumption at an LO frequency of 1 GHz.

Tab. I shows a comparison of IBFOM, OBFOM and ACFOM of this work with the state-of-the-art mixer-first receivers. The proposed receiver has the highest IBFOM even without NC cancellation due to the low power consumption of g_{m1} and g_{m2} stages. We could not reduce the power consumption of the main path drastically because of the $1/g_m$ matching [78]. With the noise cancellation, the increases in gain, IIP3 and NF have enhanced the IBFOM by more than 12 dB. [65] has the highest OBFOM because of the high $\text{OB-IIP3}_{\text{sat.}}$ and low dynamic power consumption. The ACFOM of the current receiver is also enhanced by 17 dB with NC.

6

Conclusion

Contents

6.1 Conclusion

In this thesis, switched-capacitor based integrated circuits were proposed for (a) transmitter leakage and (b) transmitter echo cancellation in an FD receiver. The proposed modules included a transformer-less duplexer for transmitter leakage cancellation and a passive continuous vector modulator for transmitter echo cancellation. Both of these SI canceling circuits were passive and were compatible with passive mixer-first receivers. The proposed transformer-less duplexer consisted of two quarter-wavelength transmission lines and an N-path balun BPF. The widely tunable balun used two 2-port N-path BPFs with embedded quadrature phase-shifting to achieve the single-ended to differential conversion. The proposed balun can be used in a wide variety of applications, including software-defined radios, phased array systems, and MIMO communication systems. In this work, N-path balun was utilized in the implementation of the transformer-less duplexer. Due to the inherent property of N-path filters, the duplexer provided an additional advantage of tunable high-Q filtering. One disadvantage of the proposed duplexer was that it discretized the received signal amplitude. Further investigations are needed to understand the behavior of the duplexer when antenna and balance ports are unbalanced.

A frequency-agile in-band FD receiver based on a switched-capacitor continuous-mode vector modulator was presented to mitigate the transmitter echo. The passive vector modulator presented in this work provided simultaneous downmixing, attenuation, and phase-shifting and generated a baseband canceller signal for SI cancellation. Though the proposed vector modulator downmixer was mainly to cancel the transmitter echo in the receiving path, it can also cancel the transmitter leakage into the receiver. The proposed vector modulator was highly linear because of passive switches and capacitors. Moreover, the vector modulator did not contribute much noise to the system. The IIP3 and NF of the system were mainly limited by the receiving path rather than the canceling path. To improve the performance of the proposed FD receiver, the baseband stage of the mixer-first receiver should have high IIP3 and have low NF. The TIA can impose tradeoff between IB-IIP3 and NF in an N-path mixer-first receiver. A second-order baseband noise-canceling scheme was proposed to break the tradeoffs. In the proposed receiver, each performance metric can be independently tuned with the help of different sub-blocks in the TIA. The prototype receiver presented in this work achieved the highest IB-SFDR and the highest close-in OB- SFDR with the lowest static power consumption among the recently published mixer-first receivers.

6.2 Future scope

The study presented in this dissertation leads to several topics for future research.

The transformer-less duplexer presented in this work is designed with an N-path balun and two $\lambda/4$ transmission lines. The proposed duplexer can operate at mm-wave frequencies similar to mm-wave circulator using spatio-temporal conductivity modulation [90]. Circulator achieves broadband non-reciprocal gyrator functionality over theoretically infinite bandwidth. While comparing to the typical operation of an N-path filter, spatio-temporal conductivity modulation requires only four-phase 50% duty-cycle clocking at frequencies significantly lower than the operation frequency, enabling scaling to mm-waves. The vector modulator presented in this work can provide the amplitude and phase tunability but not the group delay tunability as required for an SI canceller. This lack of delay adjustment caused the poor cancellation of SI in the presence of large group delays. Moreover, group delays can severely affect the cancellation in case of over-the-air testing. Integrated true-time delay cells such can be used in front of the proposed vector modulator to realize a broadband SI canceller. In N-path filters, group delay can be tuned by changing the order of the lowpass filter between two switches. Though the proposed vector modulator downmixer is mainly to cancel the transmitter echo in the receiving path, it can also cancel the transmitter leakage into the receiver. Transmitter leakage could be significant at mm-wave frequencies. The switched capacitor vector modulator presented in this work uses a sampling circuit with a very low time constant and hence is capable of working even at mm-wave frequencies provided the availability of the eight clock phases. In the proposed second-order TIA, the zero location can not be changed once the filter's quality factor is decided. Hence, it affects the steep roll-off and out-of-band IIP3. This is mainly due to the Rauch filter design. It is not possible to achieve a high-quality factor for the filter while keeping the zero far-way from the location of poles. The impedance roll-off can be further improved by incorporating a shunt-notch element [69] and [85]. The proposed baseband noise-canceling scheme can be extended to other higher-order TIAs.

A

Comparison Between opamp based TIA and OTA based TIA.

Contents

Fig. A.1(a) shows the equivalent LTI model of an N-path mixer-first receiver. A thorough analysis of this model can be studied in [52]. The baseband resistor γR_B can be replaced by a TIA. The network in-front of TIA is replaced by its equivalent Thevenin network, as shown in Fig. A.1(a). Fig. A.1(b) shows two possible implementations of a TIA using an opamp and an OTA. The non-linear models of the opamp and the OTA are considered to evaluate the IIP3 of the receiver. Even order terms can be ignored in the case of differential amplifiers. The switches are assumed to be linear. The only source of non-linearity is either opamp or OTA. The noise sources are switch (R_{sw}), shunt resistor (R_{sh}) and TIA. The following subsections discuss the trade-offs among input-match, linearity, noise figure and power for opamp and OTA based TIAs.

A.1 opamp based TIA

A.1.1 Dependence of Linearity on Input-match

The equivalent Thevenin network is used to compute first and third-order terms of the voltage gain, as shown in Fig. A.1(a). A detailed analysis is shown in Appendix B to evaluate these terms. Based on these terms, IIP3 of the receiver can be calculated and is given by

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\frac{\left[1+\frac{R_{Th}}{\gamma R_B}\right]^3}{\left[1+\frac{R_{Th}}{\gamma R_B(1+a1)}\right]}\right|}.\frac{R_a}{R_{Th}}, \tag{A.1}$$

where, (A.2)

$$R_B = \frac{R_F}{1+a_1}, R_a = R_s + R_{sw} \text{ and } R_{Th} = R_{sh}||R_a.$$

(A.1) depicts that IIP3 is inversely proportional with R_B. When the opamp is operating in open-loop ($R_F = \infty$), IIP3 of the receiver is given by

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{a_1}{a_3}\right|}.\frac{R_a}{R_{Th}} \tag{A.3}$$

The IIP3 of the receiver is normalized with respect to IIP3 obtained in open-loop from (A.1) and (A.3). The normalized IIP3 can be written as

$$\text{IIP3}_{\text{Norm.}} = \sqrt{\left|\frac{\left[1+\frac{R_{Th}}{\gamma R_B}\right]^3}{\left[1+\frac{R_{Th}}{\gamma R_B(1+a1)}\right]}\right|} \tag{A.4}$$

Assume open-loop gain (a_1) is sufficiently large so that $\frac{R_{Th}}{\gamma R_B(1+a_1)} \ll 1$. (A.4) can be written as

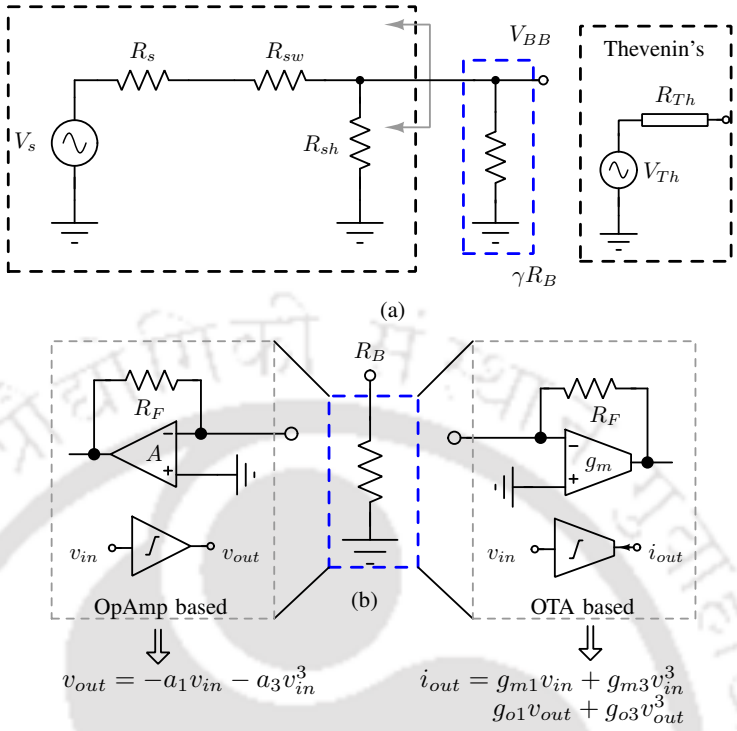


Figure A.1: (a) Equivalent LTI model of an N-path mixer-first receiver. (b) Implementation of TIA using opamp and OTA.

$$\text{IIP3}_{\text{Norm.}} \approx \sqrt{\left|\left[1 + \frac{R_{Th}}{\gamma R_B}\right]^3\right|} \tag{A.5}$$

The value of baseband resistor R_B can be calculated from [52] to achieve the input match. It comes out to be 250 Ω for N=4. From (A.5), When R_B=250 Ω, the normalized IIP3 is approximately 8.2 dB. In other words, If the IIP3 of the opamp is 0 dBm in open-loop, one can never achieve more than 8.2 dBm of IIP3 for an input-matched receiver. There is a tradeoff associated with input-match and linearity. (A.5) is verified in simulations for 4-path mixer-first receiver. Fig. A.2(a) shows a comparison between simulated and analytical (A.5) normalized IIP3 of the receiver for different R_B values. In this simulation, the following parameters are used: $R_{sw} = 5\ \Omega$, $a_1 = 100$ and $a_3 = 300$.

A.1.2 Degree of freedom for noise figure and power

From [52], noise factor of the receiver is given by

$$NF = 1 + \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left[\frac{R_a}{R_{sh}}\right]^2 + \gamma\frac{R_F}{R_s}\left[\frac{R_a}{\gamma R_F}\right]^2 + \gamma\frac{v_{n,A}^2}{4KTR_s}\left[\frac{R_a}{\gamma R_F} + \frac{R_a + R_{sh}}{R_{sh}}\right]^2, \tag{A.6}$$

where $v_{n,A}$ is input referred noise voltage of the opamp. Fig. A.2(b) shows the simulated and

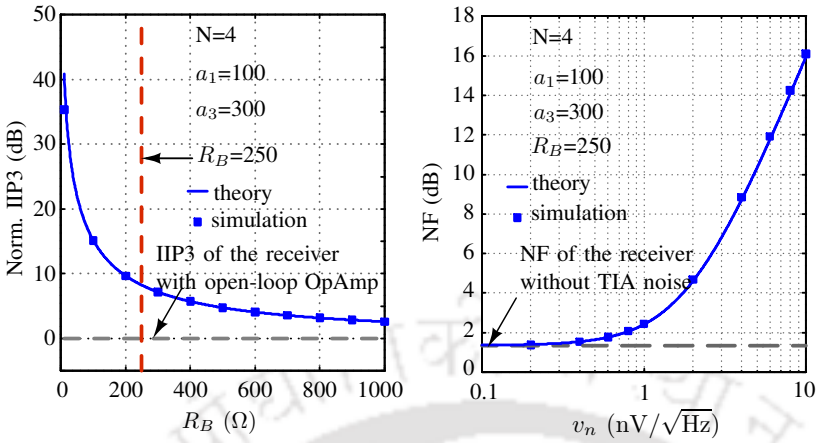


Figure A.2: Comparison of simulated and analytical (a) Normalized IIP3 and (b) NF of the receiver using opamp based TIA.

analytical (A.6) noise figure of the receiver for different $v_{n,A}$. From Fig. A.1(b), the noise figure of the receiver is mainly decided by the noise voltage of the opamp. One has to increase the bias current to reduce the noise of the opamp. Fig. A.2(b) shows that the desired NF (close to the dashed line in Fig. A.2(b)) can be achieved by using an opamp based TIA while having input-match. In this simulation, the following parameters are used: $R_{sw} = 5\ \Omega$, $a_1 = 100$, $R_B = 250\ \Omega$.

A.2 OTA based TIA

A.2.1 Degree of freedom for Linearity

Apart from the opamp, a shunt feedback OTA can be used as baseband resistor R_B in the mixer-first receivers. Fig. A.1(a) shows non-linear model of the OTA. This model include non-linearities due to transconductance and output conductance, where g_{m3} and g_{o3} are third-order terms of transconductance and output conductance, respectively. IIP3 of the receiver can be computed in a similar way as in the previous subsection and is given by

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\left[1+\frac{R_{Th}}{\gamma R_F}+\frac{1}{g_{o1}R_F}(1+\frac{g_{m1}R_{Th}}{\gamma})\right]^3}{\left[\frac{g_{m3}}{\gamma}(1+\frac{1}{g_{o1}R_F})^3+\frac{g_{o3}}{\gamma}(\frac{1}{g_{o1}R_F}-\frac{g_{m1}}{g_{o1}})^3\right]}\right|} \times \sqrt{\left|\frac{(1-g_{m1}R_F)}{(\gamma R_F+R_{Th})}\right|}.\frac{R_a}{R_{Th}} \tag{A.7}$$

The input resistance of an OTA based TIA is approximately $\frac{1}{g_{m1}}$ when $R_F g_{o1} \ll 1$. Therefore, input-match can be achieved by keeping $g_{m1} = \frac{1}{R_B}$. Equation (A.7) depends on various design parameters such as $g_{m1}, g_{m3}, g_{o1}, g_{o3}$ and R_F. From (A.7), one can adjust IIP3 of the receiver by changing R_F

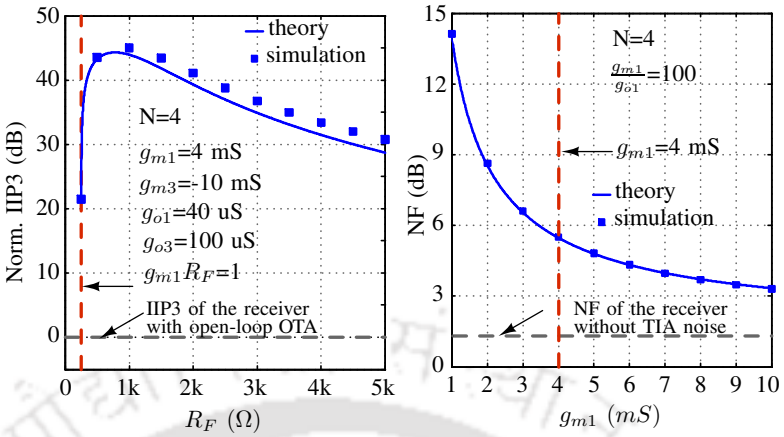


Figure A.3: Comparison of simulated and analytical (a) Normalized IIP3 and (b) NF of the receiver using OTA based TIA.

without affecting the input-match. Assuming $R_F \ll \frac{1}{g_{o1}}$, (A.7) can be written as

$$\text{IIP3} \approx \sqrt{\frac{4}{3}\left|\frac{\left[1+\frac{g_{m1}R_{Th}}{\gamma}\right]^3}{\left[\frac{g_{m3}}{\gamma}-\frac{g_{o3}}{\gamma}(g_{m1}R_F)^3\right]}\right|} \times \sqrt{\left|\frac{(1-g_{m1}R_F)}{(\gamma R_F+R_{Th})}\right|}.\frac{R_a}{R_{Th}} \tag{A.8}$$

When the OTA is operating in open-loop ($R_F = \infty$), IIP3 of the receiver can be computed from (A.7) and is given by

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{g_{m1}}{\left[g_{m3}-g_{o3}(\frac{g_{m1}}{g_{o1}})^3\right]}\right|}.\frac{R_a}{R_{Th}}$$

The IIP3 of the receiver is normalized with respect to IIP3 obtained in open-loop case from (A.8) and (A.9). The normalized IIP3 can be written as

$$\text{IIP3}_{\text{Norm.}} \approx \sqrt{\left|\frac{\left[1+\frac{g_{m1}R_{Th}}{\gamma}\right]^3}{\left[\frac{g_{m3}}{\gamma}-\frac{g_{o3}}{\gamma}(g_{m1}R_F)^3\right]}\right|} \times \sqrt{\left|\frac{(1-g_{m1}R_F)\left[g_{m3}-g_{o3}(\frac{g_{m1}}{g_{o1}})^3\right]}{g_{m1}(\gamma R_F+R_{Th})}\right|} \tag{A.9}$$

Equation (A.9) is verified in simulations for 4-path mixer-first receiver. Fig. A.3(a) shows a comparison between simulated and analytical (5) normalized IIP3 of the receiver for different R_F values. In this simulation, the following parameters are used: $R_{sw} = 5\ \Omega$, $g_{m1} = 4$ mS, $g_{m3} =$ -10 mS, $g_{o1} = 40$ uS and $g_{o3} = 100$ uS. Fig. A.3(a) shows that it is possible to have a wide range of IIP3 for the receiver using the OTA based TIAs. From Fig. A.2(a) and Fig. A.3(a), one can get higher IIP3 with an OTA rather than an opamp for the same input-match.

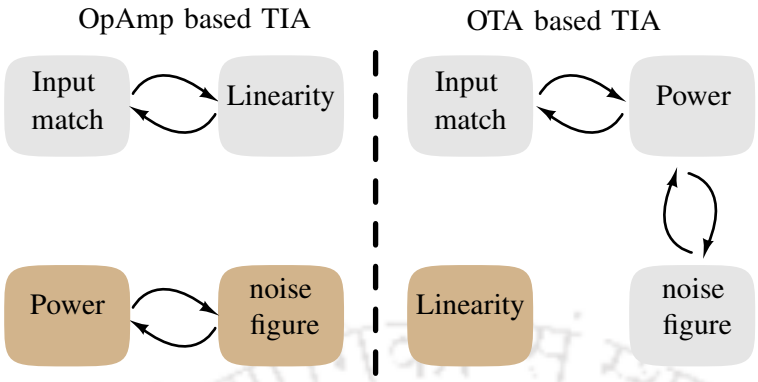


Figure A.4: Tradeoffs in the mixer-first receivers using an opamp based or an OTA based TIA.

A.2.2 Dependence of noise figure and power on input-match

From [78], the noise factor of the receiver is given by

$$NF = 1 + \frac{R_{sw}}{R_s} + \frac{R_{sh}}{R_s}\left[\frac{R_a}{R_{sh}}\right]^2 + \frac{\gamma R_F}{R_s}\frac{1}{G_N^2} + \gamma\frac{\overline{i^2_{n,g_{m1}}}}{4KTR_s}\left[\frac{R_F + \frac{R_{Th}}{\gamma}}{1 - g_{m1}R_F}\right]^2\left[\frac{R_{sh} + R_a}{R_{sh}}\right]^2. \quad \text{(A.10)}$$

where, $\overline{i^2_{n,g_m}}$ is the output noise current of the OTA, and is given by $\overline{i^2_{n,g_m}}$ = 4KT NEFg_{m1}, where NEF is a noise excess factor. A MOSFET has NEF of 2/3 in strong inversion (closer to 3/2 in real). G_N is the voltage gain of the receiver which is given by

$$G_N = \left[\frac{1 - g_m R_F}{1 + \frac{g_m R_{Th}}{\gamma}}\right]\left[\frac{R_{sh}}{R_{sh} + R_a}\right]$$

Fig. A.3(b) shows the simulated and analytical (A.10) noise figure of the receiver for different g_{m1}. From (A.11), When g_{m1}=4 mS and R_F=1 KΩ, the NF of the receiver is close to 5.5 dB. Fig. A.3(b) shows that it is difficult to achieve sub 3-dB NF with an OTA based TIA. Therefore, there is trade-off associated with input-match and NF. In this simulation, the following parameters are used: R_{sw} = 5 Ω, R_F = 2.5 kΩ and $\frac{g_{m1}}{g_{o1}}$ = 100.

A.3 Challenges in breaking the tradeoffs

An N-path mixer first receiver can be implemented using an opamp based or an OTA based TIA. The previous subsections discuss the merits and demerits of these two designs in terms of input-match, linearity, noise figure and power. Fig. A.1 shows trade-offs in the mixer-first receivers. The main challenge comes in the circuit level design. All these parameters are indirectly linked with each other because of the analog design octagon. For example, a receiver designed using opamp based TIA

can relax the noise figure and power irrespective of the input match. Even a slight change in power consumption of opamp may alter the linearity, which in turn will affect the input match. It is difficult to break all these trade-offs, as they all depend on a single block.

B

IIP3 Of A Mixer-First Receiver With Shunt-Feedback TIA

Contents

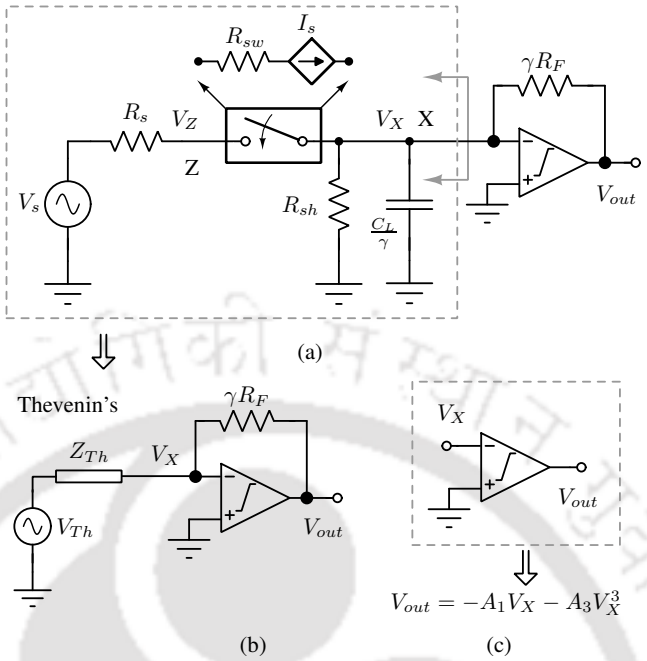


Figure B.1: (a) Equivalent LTI model of an N-path mixer-first receivers. (b) Equivalent Thevenin model of dotted portion shown in (a). (c) A non-linear model of the opamp.

B.1 General considerations:

The output voltage (V_{out}) of a non-linear system for a given input voltage (V_s) can be represented as the following polynomial expression.

$$V_{out} = \beta_1 V_s + \beta_2 V_s^2 + \beta_3 V_s^3 + ... + \beta_n V_s^n, \tag{B.1}$$

where β_1, β_2, β_3, and β_n are the Taylor series coefficients of the output. Here,

$$\beta_n = \frac{1}{n!}\left(\frac{\partial V_{out}}{\partial V_s}\right)_{V_s=0}. \tag{B.2}$$

The IIP3 of the system defined by (B.1) is given by [83]

$$\text{IIP3} \approx \sqrt{\frac{4}{3}\frac{\beta_1}{\beta_3}}. \tag{B.3}$$

B.2 IIP3 of a mixer-first receiver with a shunt-feedback TIA:

Fig. B.1(a) shows the equivalent LTI model of an N-path mixer-first receiver with a shunt-feedback TIA. In Fig. B.1(a), R_s is the source resistance, R_{sw} is the on-resistance of switches, R_{sh} accounts for

the power loss due to the up-conversion of the input signal, and γ represents a constant that depends on the number of paths [52]. The network in-front of the TIA is replaced by its equivalent Thevenin network, as shown in Fig. B.1(b). The opamp is assumed to have a third-order non-linear transfer characteristics as shown in Fig. B.1(c). The output voltage (V_{out}) of the opamp for a differential input voltage (V_X) is given below.

$$V_{out} = -A_1 V_X - A_3 V_X^3, \tag{B.4}$$

where A_1 and A_3 are first-order and third-order Taylor series coefficients. The switches are also considered to be non-linear. A non-linear switch can be modeled as a series combination of its on-resistance and a dependent current source as shown in Fig. B.1(a) [86]. Let the output current of the MOSFET switch (I_s) is given by

$$I_s = \alpha_1 V_s + \alpha_3 V_s^3, \tag{B.5}$$

where α_1 and α_3 are linear and third-order conductances of the MOSFET switch, respectively. The voltage V_X at the node X, shown in Fig. B.1(a), is

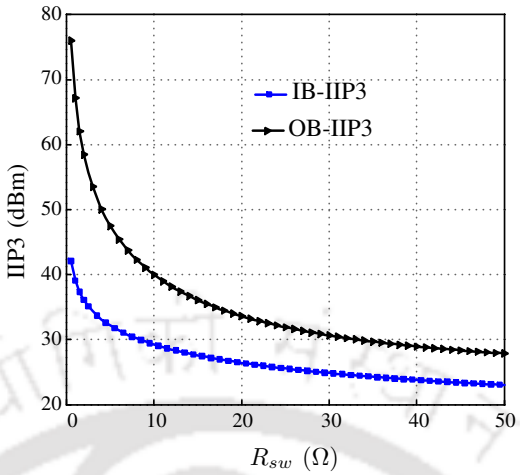
$$V_X = \frac{\gamma R_F V_{Th} + Z_{Th} V_{out}}{\gamma R_F + Z_{Th}}, \tag{B.6}$$

where

$$V_{Th} = Z_{sh}[\alpha_1 V_s + \alpha_3 V_s^3], Z_{sh} = R_{sh} || \frac{\gamma}{j\omega C_L},$$
$$Z_{Th} = R_{Th} || \frac{\gamma}{j\omega C_L} \quad \text{and} \quad R_{Th} = R_{sh} || R_a.$$

From (B.4) and (B.6), the output voltage can be written as

$$V_{out} = -A_1 \left(\frac{\gamma R_F V_{Th} + Z_{Th} V_{out}}{\gamma R_F + Z_{Th}} \right) - A_3 \left(\frac{\gamma R_F V_{Th} + Z_{Th} V_{out}}{\gamma R_F + Z_{Th}} \right)^3. \tag{B.7}$$



For IB-IIP3:-

$$\alpha_1 = \frac{1}{R_s+R_{sw}+R_{sh}}$$

$$\alpha_3 = \frac{-[(R_{sw}+R_{sh})(R_s+R_{sh})+R_{sh}R_{sw}]R_{sw}(R_{sw}+2R_{sh})}{2V_{OD}^2(R_s+R_{sw}+R_{sh})^5}$$

For OB-IIP3:-

$$\alpha_1 = \frac{1}{R_s+R_{sw}}$$

$$\alpha_3 = \frac{-R_{sw}^3 R_s}{2V_{OD}^2(R_s+R_{sw})^5}$$

Figure B.2: Theoretical (a) IB-IIP3 and (b) OB-IIP3 of the receiver (considering only the non-linearity of switches).

From (B.2) and (B.7), β_1 and β_3 can be computed.

$$\beta_1 = \frac{-Z_{sh}A_1\alpha_1}{1+\frac{Z_{Th}}{\gamma R_B}}, \tag{B.8}$$

$$\beta_3 = -\frac{Z_{sh}A_1\alpha_3}{1+\frac{Z_{Th}}{\gamma R_B}} - \frac{Z_{sh}^3\alpha_1^3A_3(1+\frac{Z_{Th}}{\gamma R_F})}{(1+\frac{Z_{Th}}{\gamma R_B})^4}, \tag{B.9}$$

$$\text{where } R_B = \frac{R_F}{1+A_1}.$$

The IIP3 of the mixer-first receiver can be computed from (B.3), (B.8) and (B.9), and is given by

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\left[\frac{\alpha_3}{\alpha_1} + \frac{Z_{sh}^2\alpha_1^2A_3(1+\frac{Z_{Th}}{\gamma R_F})}{A_1(1+\frac{Z_{Th}}{\gamma R_B})^3}\right]^{-1}\right|}. \tag{B.10}$$

If the oapmp has a large gain (A_1) then $\frac{Z_{Th}}{\gamma R_B(1+A_1)} \ll 1$, and (B.10) can be reduced to

$$\text{IIP3} \approx \sqrt{\frac{4}{3}\left|\frac{1}{(\eta_{\text{sw}})^{-1}+(\eta_{\text{TIA}})^{-1}}\right|}, \tag{B.11}$$

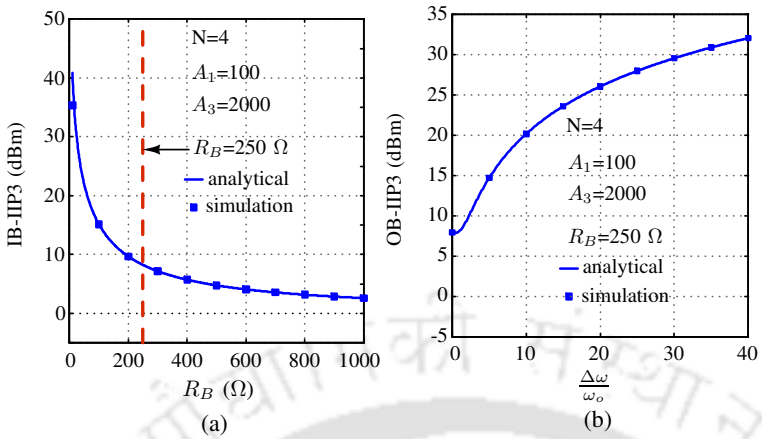


Figure B.3: Comparison of simulated and analytical (a) IB-IIP3 and (b) OB-IIP3.

where

$$\eta_{\text{sw}} = \frac{\alpha_1}{\alpha_3}, \quad \eta_{\text{TIA}} = \frac{A_1(1+\frac{Z_{Th}}{\gamma R_B})^3}{A_3 Z_{sh}^2 \alpha_1^2}.$$

B.3 Computing α_1 and α_3 using the square-law model:

Using the square-law model of MOSFET, the switch current I_s when it is ON is

$$I_s = \mu_n C_{ox} \frac{W}{L}\big((V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\big) \tag{B.12}$$

From Fig. B.1(a), (B.12) can be written as

$$I_s = \mu_n C_{ox} \frac{W}{L}\left((V_{DD} - V_{th} - V_Z)(V_X - V_Z) - \frac{(V_X - V_Z)^2}{2}\right), \tag{B.13}$$

where

$$V_Z = V_s - I_s R_s \text{ and } V_X = I_s Z_{sh}. \tag{B.14}$$

From (B.2), (B.13) and (B.14) linear (α_1) and third-order (α_3) coefficients of switches are

$$\alpha_1 = \frac{1}{R_s + R_{sw} + Z_{sh}}, \tag{B.15}$$

$$\alpha_3 = \frac{-[(R_{sw} + Z_{sh})(R_s + Z_{sh}) + Z_{sh}R_{sw}]}{2V_{OD}^2(R_s + R_{sw} + Z_{sh})^5} \times R_{sw}(R_{sw} + 2Z_{sh}), \tag{B.16}$$

where V_{OD} is the overdrive voltage $(V_{DD} - V_{th})$ when the switch is ON.

B.4 Simplified expressions of IB-IIP3 and OB-IIP3:

Considering only the non-linearity of switches ($A_3 = 0$), the IIP3 of the mixer-first receiver is given by

$$\text{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{B.17}$$

Using (B.17), the theoretical IB-IIP3 and OB-IIP3 are plotted in Fig. B.2. One can infer from Fig. B.2 that the typical IIP3 of passive MOSFET mixers is greater than +20 dBm. Typical IIP3 of the baseband amplifier is much less than +20 dBm. Hence, over the frequency range in which the TIA affects the receiver performance (IB and close-in OB), the switch non-linearity can be neglected ($\eta_{\text{sw}} \gg \eta_{\text{TIA}}$). The reduced expression of the IIP3 is

$$\text{IIP3} \approx \sqrt{\frac{4}{3}\left|(\eta_{\text{TIA}})\right|}, \tag{B.18}$$

where

$$\eta_{\text{TIA}} = \frac{A_1}{A_3}\left[\frac{\left(1+\frac{R_{Th}}{\gamma R_B}\right)^2 + \left(\frac{\Delta\omega}{\omega_o}\right)^2}{1+\left(\frac{\Delta\omega}{\omega_o}\right)^2}\right]^{\frac{3}{2}}\left(\frac{R_a}{R_{Th}}\right)^2 \times \left[1+\left(\frac{\Delta\omega}{\omega_o}\right)^2\right],$$

where ω_o is the 3-dB frequency $\left(\omega_o = \frac{\gamma}{R_{Th}C_L}\right)$ and $\Delta\omega$ is the offset from the center frequency. In the passband, $Z_{Th} \approx R_a||R_{sh}$ and $\Delta\omega = 0$. The IB-IIP3 of the receiver is given by

$$\text{IB}-\text{IIP3} \approx \sqrt{\frac{4}{3}\left|\frac{A_1}{A_3}\right|\left[1+\frac{R_{Th}}{\gamma R_B}\right]^3} \times \frac{R_a}{R_{Th}}. \tag{B.19}$$

The equations (B.18) and (B.19) are verified by simulating a receiver with a non-linear model of the opamp. Fig. B.3(a) shows the variation of IB-IIP3 with R_B. Fig. B.3(b) shows the variation of OB-IIP3 with $\Delta\omega/\omega_o$. In this simulation, the following parameters are used: $R_{sw} = 5\ \Omega$, $C_L = 20$ pF, $A_1 = 100$, $A_3 = 2000$ and $R_B = 250\ \Omega$.

When we move far way from the 3-dB frequency ($\omega \to \infty$, ${\eta_{\text{TIA}}}^{-1} \to 0$), the OB-IIP3 of the receiver is limited by the mixer-switches [79]. In this case, the OB-IIP3 of the receiver is dominated by the non-linearity of switches only.

$$\text{OB}-\text{IIP3}_{\text{sat.}} \approx \sqrt{\frac{4}{3}|\eta_{\text{sw}}|} \approx \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}, \tag{B.20}$$

where α_1 and α_3 can obtained from (B.15) and (B.16) resepctively.

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Journal Publications

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- P. K. Sharma and N. Nallam, "Linearity and NF Tradeoff in Input-Matched N-Path Mixer-First Receivers with Shunt-Feedback TIAs," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2019, pp. 1-4.
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- P. K. Sharma and N. Nallam, "A Transformer-less Duplexer with Out-of-Band Filtering for Same-Channel Full-Duplex Radios," in Proc. IEEE Int. Symp. Circuits Syst. (ISCAS), May 2017, pp. 1-4.

Patents

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