

ABSTRACT

The scope of this thesis work is motivated by implementation challenges of designing low power analog circuits for front-end amplifiers and area-efficient spike detector for neural recording microsystems. The key challenge in the design of neural amplifier is large input DC offsets associated with the electrodes. Neural signals superimposed on these offsets saturates the amplifier's front-end. One of the solution is to improve input linear range in order to accommodate offset voltages of up to few tens of mV. First part of the thesis proposes a sub-threshold OTA topology for the development of a nano-power local field potential (LFP) recording amplifier with a high dynamic range specification. This work also addresses the design criteria of power dissipation, area consumption, and the noise performance.

The second part of the thesis presents a low-power neural recording front-end amplifier with a band programmability feature for separation of extra-cellular neural spike and LFP signal. This allows for the preconditioning of neural signals for delivery to subsequent spike detection system. An improved version of neural recording amplifier configured as LFP amplifier is also presented. The amplifier design focusses on minimizing low cut-off frequency for filtering out large DC offset and low frequency noise. The performance of amplifier is validated by implementing the LFP recording amplifier integrated circuit in a commercially available 1.5 V 180 nm CMOS process. The measured results shows the amplifier to be programmable for different mid-band gains while achieving a sub-10 mHz cut-off frequency for low noise neural data processing.

Third part of this thesis proposes a novel spike detection algorithm capable of estimating the instantaneous neural background noise. The objective is to develop a robust spike detection system which yields a reliable performance under rapid variations of spike amplitude and firing rates. We describe an area efficient, low power subthreshold analog spike detector circuit capable of adaptively discriminating neural spikes from background noise in real-time. The circuit implementation focusses on achieving an optimal performance in terms of energy-efficiency and compactness. Simulations are conducted which establishes the robustness of the proposed technique in terms of detection performance when compared to state-of-the-art. The algorithm implemented in analog CMOS circuit leads to a low power consumption and occupies an area that fits well into a size of acceptable standards.

The major contributions of this thesis are as follows:

- Linearity improvement in a 1 V transconductor with a nonlinearity error of less than 0.5 % for the differential input signals of up to 1.2 V (peak-to-peak)
- A 0.8 V single-ended LFP amplifier with a THD of 1% @20.2 mVpp having layout area of 0.098 mm² while consuming 68.4 nW of power.
- A 1.5 V programmable neural recording amplifier configured for LFP with a cut-off frequency of 3 mHz having layout area of 0.086 mm² and power dissipation of less than 10 μ W.
- A 0.8 V automatic real-time spike detector with an adaptive threshold estimation with power dissipation of 4.2 μ W and a layout area of 0.016 mm².

Keywords: *Linearity, operational transconductance amplifier, Dynamic range, Action potential, Local field potential, ultra-low power circuit design, neural amplifier, weak inversion, Spike detection, nonlinear energy operator, Extracellular neuronal recordings, Spike train, Threshold selection.*