INDIAN INSTITUTE OF TECHNOLOGY GUWAHATI
SHORT ABSTRACT OF THESIS

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Thesis Title: Low Complexity Distributed Arithmetic Based Pipelined VLSI Architectures for LMS Adaptive Filters

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SHORT ABSTRACT

Least-mean-square (LMS) algorithm is widely used in system identification, channel equalization, noise cancellation, and several other areas of digital signal processing due to its simplicity and ease of implementation. In most of the cases, LMS algorithm is not employed directly, rather a combination of LMS units in parallel or in series or in block is used to obtain the desired performance. For instance, the parallel combination of two LMS adaptive filters with different step-size has fast convergence and low steady-state error, the series combination of two LMS adaptive filters in the feedforward and the feedback topology has better performance against noise and interference, and the block implementation of LMS adaptive filters is used to realize higher order filters. Distributed arithmetic (DA) is an efficient multiplierless approach for implementation of LMS adaptive filter DA based implementations basically consist of a look-up table (LUT) followed by a shift-accumulate (SA) unit. But, the direct usage of DA for complexity reduction of the adaptive filter, especially in high-throughput applications would be challenging, since time required to access LUT and to compute SA unit is significant. The modularity feature of DA makes it amenable for implementing on field-programmable gate arrays (FPGA) and the design of application specific integrated circuit (ASIC). In this thesis, we first derived three optimal complexity pipelined architectures for LMS adaptive filter using offset-binary-coding (OBC) DA. Although it is straightforward to pre-compute and store the filter partial products in LUT for the realization of non-adaptive filter such as finite impulse response (FIR) filter using DA, problem arises while generating them using hardware elements to overcome the access time of LUT. This is because the number of hardware elements required to generate the filter partial products for LUTless design grows exponentially with filter order. To address this issue,

we implemented partial products of input samples serially by representing the filter coefficients in OBC-form. But, this produces non-OBC terms at the output during some initial clock cycles due to pipelined nature of filter, which are subsequently corrected in the error computation unit. The reason for choosing the OBC scheme in the implementation of pipelined LMS adaptive filter is to exploit the redundancies between the partial products for higher radices. This also has an advantage of less time involved in the SA unit for the computation of filter output. All the proposed architectures are extended for large order filter design with modification in the correction of non-OBC terms. Next, we applied two's complement (TC) DA to the pipelined realization of convex combination of two parallel LMS adaptive filters which greatly improves the convergence performance. Unlike conventional LMS algorithm, the combination of two LMS filter in parallel can provide fast convergence and low steady-state error by transferring the filter coefficients from one LMS unit to other. However, the computational requirements are significantly higher due to two LMS units and coefficient transfer scheme. To alleviate this problem, we employed a single DA based LMS adaptive filter with a new coefficient transfer scheme. Further reduction in computational complexity is achieved by sharing the partial products and employing bit-level coefficient update accumulators. The reduction in hardware elements is utilized to transfer the filter coefficients by switching the step-size. As a result, it enhances the filter convergence properties with an efficient criterion based on the correlation between adjacent delayed error samples. The duration of correlation between adjacent errors is then compared with a pre-defined time window in every iteration. In the sequel, an analytical expression for pre-defined time window is derived in terms of filter parameters such as filter order, coefficients wordlength and step-size. Later, we considered low-complexity DA based VLSI implementation of the adaptive filter for channel equalization problem in 5G communication system. In this work, we employed two LMS adaptive filters in series with one in the feedforward path and other in the feedback path with a decision device. The overall system is designed to achieve the throughput requirement of 5G while maintaining computational complexity relatively lower than the best existing design. The design first utilizes the pipelined implementation of non-adaptive feedback filter using OBC. It is based on the fact that when radix-size becomes equal to the wordlength of decisions, the implementation of DA based LMS adaptive filter can be made SA-less. In this design, decisions are OBC coded to derive low-complexity SA-less architecture for adaptive feedback filter. The proposed architecture pre-computes and stores the coefficients in two LUTs separated by pipelined registers for complexity reduction. Further reduction in complexity is achieved by exploiting the symmetries between the stored contents of both the LUTs. The proposed architecture is pre-speed up by two, retimed and unfolded to meet the throughput requirements of 5G. To adapt the feedback coefficients, a novel strategy is presented to update the LUT contents of both the stages by adding them with the contents of external LUT storing the decisions. The contents of decision LUT are updated before the filtering operation in every iteration. Parallel error multiplexer is employed so as to remove the effect of non-OBC terms in order to improve the convergence performance. Lastly, a low-complexity design of pipelined block LMS adaptive filter is proposed for noise cancellation in in-ear headphones applications. Here, both physical LUT and SA unit are employed, and their effects on throughput performance are compensated by

block processing. It utilizes OBC scheme for complexity reduction which stores the partial products of input samples in a LUT. The symmetries in LUT contents allowed them to split into two smaller LUTs, but requires the contents of the external register to be updated along with the error computation. The splitted LUTs are shared to compute the filter output and coefficient-increment terms in the same block iteration. A novel strategy is developed to update the LUT contents in fewer number of clock cycles as compared to the best existing design. To validate the performance of the proposed architectures, ASIC and FPGA implementations are carried out to estimate area, power, throughput, number of flip-flops and slice LUTs.